MODEL PCL-818H

High Performance
Data Acquisition Card
With Programmable Gain

PCL-818H High Performance
Data Acquisition Card
With Programmable Gain

USER'S MANUAL

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CHAPTER 1. GENERAL INFORIVIATION

1.1. Introduction

The PCL-818H is a high performance, high speed, multi-function data acquisition card with **programmable gain** for the IBM PC/XT/AT or compatible computer. The high-end specifications of this full-size card and complete software support make it ideal for a wide range applications in the industrial and laboratory environment such as data acquisition, process control, automatic testing and factory automation.

1.1.1. Key Features

The key features of this interface control card include:

- A switch-selectable analog input channel configuration of either 16 single-ended or 8 differential inputs.

- An industrial standard 12 bit successive approximation A/D converter is used to convert the analog inputs. The highest A/D sampling rate is 100 KH7. in DMA mode.

- Remote programmable analog input-range setting with software control. Each channel has its own range setting, and this setting is stored in an on-board RAM.

- Software selectable analog input ranges.

  Bipolar ±0.625 V, ±1.25 V, ±2.5 V, ±5 V, ±10 V.
  Unipolar 0 to ~1.25 V, 0 to +2.5 V, 0 to +5 V, 0 to +10 V.
- The analog input-range control codes are stored in an on-board RAM. This feature enables the PCL-818H to change the range for each channel automatically when channel switching without CPU programming of the PC.

- Three A/D trigger modes: Software trigger, programmable pacer trigger and external pulse trigger.

- A/D conversion data can be transferred by program control, interrupt handler routine or DMA transfer.

- An Intel 8254 Programmable Timer/Counter provides pacer (trigger pulses) at rates from 2.5 MHz to 0.00023 Hz (71 minutes/pulse). The time base is switch selectable: 10 MHz or 1 MHz. One 16-bit counter channel is reserved for user configuration applications.

- One 12 bit monolithic multiplying D/A output channel. An output range of 0 V to -t5 V (+10V) can be generated by using the on-board -5 V (-10 V) reference. An external AC or DC reference can also be used to generate other D/A output ranges.

- 16 digital input and 16 digital output channels, all of which are TTL/DTL compatible.

1.1.2. Expansion Capabilities

To complement the powerful features of the PCL-818H, the versatility of the card can be further enhanced with the use of any of the optional daughter boards listed below:

PCLD-789

Amplifier/Multiplexer Board. This powerful front-end analog input-signal conditioning card can multiplex 16 differential inputs to one A/D input channel. A high grade instrumentation amplifier provides switch selectable gains of 0.5, 1, 2, 10, 50, 100, 200, 1000 or user definable.

PCLD-788

Relay Multiplexer Board. This relay board can multiplex 16 differential inputs to one analog output channel, and offers isolated, break-before-make, high voltage switching with CJC circuit for thermocouple measurements.

PCLD-787

8-channel simultaneous sample and hold front-end board. It allows up to eight analog inputs to be acquired simultaneously with less than 30 ns of channel-to-channel sample time uncertainty.

PCLD-786

AC/DC Power SSR and Relay Driver Board. This board provides eight channels of opto-isolated solid state relay modules plus an additional eight external relay driver outputs.

PCLD-785/885

Relay Output Board. PCLD-785 provides 16 SPDT relays, and PCLD-885 provides 16 SPST power relays all of which may be driven by the 16 bit digital output channels of the PCL-818H.

PCLD-782

Isolated D/I Board. This 16-channel opto-isolated digital input board provides an easy way to input digital signals to the PCL-818H.

PCLD-780

Wiring Terminal Board. This board is designed for easy analog and/or digital I/O connections.

PCI,D-779

Eight channel relay, isolated multiplexer and amplifier board. It offers multi-channel temperature measurements when connected to a PC-LabCard.

PCLD-770/7701/7702

PCLD-770 is a signal conditioning module carrier board. With the PCLD-770 board, you can configure your signal-conditioning module requirements, such as the PCLD-7701 isolated amplifier, or the PCLD-7702 amplifier with I/V source, etc.

PCLD-SB16

This module carrier board is equipped with 16 channels of SE-series input and/or *output* modules which provide a complete solution for signal conditioning applications.

1.1.3. Software Support

The PCL-818H also provides a powerful and easy-to-use software driver whose functions can be accessed by referring to a user-defined Parameter Table. With these driver functions your application programming becomes much easier, especially when you want to use some of the sophisticated features available from the PCL-818H, such as interrupt or DMA data transfer.

To provide PCL-818H users with more application support, a variety of excellent third-party application software packages can work with the PCL-818H. Currently, the following software packages support the PCL-818H:

DADiSP

Spreadsheet software for off-line data analysis and digital signal processing from DSP Development Corp.

LABTECH NOTEBOOK

Integrated data acquisition software with real time analysis, display and process control from Laboratory Technologies Corp.

LABTECH ACQUIRE

Low cost data acquisition software from Laboratory Technologies Corp.

PC-LabDAS

Turn-key, menu driven, general purpose data acquisition package from Advantech.

PC-Scope

Storage-oscilloscope emulation software which turns your PC into a high-quality storage scope. This package is also from Advantech.

SNAP-MASTEK for Microsoft Windows

A PC-based data-acquisition, analysis and display software tool that works with Microsoft Windows. It is the first Windows-based package that allows control of sensors, transducers, actuators and signal conditioners as part of the data-acquisition system; from HEM Data Corporation.

GENESIS

The first icon-based process-control software from ICONICS, Inc. It transforms the IBM PC into a multi-function CAD workstation for graphically creating, simulating, and executing real-time data acquisition and process control strategies.

Contact your local PC-LabCard representatives for more information about software package validity.

1.2. Product Specifications

1.2.1. Analog Input (A/D Converter)

Channels : 16 single-ended or 8 differential, switch selectable.

Resolution : 12 bits.

Input ranges (in $Volts_{DC}$)	:	Bipolar : ±0.625, ± 1.25, ±2.5, ±5, ±10 Unipolar: 0 to +1.25, 0 to +2.5, 0 to +5, 0 to +10. (All input ranges are software programmable)
Overvoltage	:	Continuous ±30 V max.
Conversion type	:	Successive approximation.
Conversion rate	:	100KHz max.
Accuracy	:	±(0.01% of reading), ±l bit.
Linearity	:	± 1 bit.
Trigger mode	:	Software trigger, on-board programmable pacer trigger or external trigger.
Ext. trigger	:	TTL compatible: the load is 0.4 mA max. at 0.5 V and -0.05 mA max. at 2.7 V.
Data transfer	:	Program, interrupt or DMA.

1.2.2. Analog Output (D/A Converter)

Channels	:	1 channel.
Resolution	:	12 bits.
Output Range	:	0 to +5 (+10) V with on-board -5 (-10) V reference. Max. ±10 V with external DC or AC reference.
Reference	:	Internal: -5 V or -10 V External DC or AC : ±10 V max.
Conversion type	:	12 bit monolithic multiplying.

Linearity	:	±0.5 bit.
Output drive	:	±5mA max.
Settling time	:	5 microseconds.

1.2.3. Digital Input

Channel	:	16 bits.
Level	:	TTL compatible.
Input voltage	:	Low -- 0.8 V max. High -- 2.0 V min.
Input load	:	Low -- 0.4 mA max. at 0.5 V. High -- 0.05 mA max, at 2.7 V.

1.2.4. Digital Output

Channel	:	16bits.
Level	:	TTL compatible.
Output voltage	:	Low ~ Sink 8 mA at 0.5 V max. High -- Source -0.4 mA at 2.4 V min.

1.2.5. Programmable Timer/Counter

Device	:	Intel 8254 or equivalent.
Counters	:	3 channels, 16 bit. 2 channels are permanently configured as programmable pacers; 1 channel is free for user's application.
Input, gate	:	TTL/CMOS compatible.

Time base :

Pacer (channels 1 and 2)	:	10 MHz or 1 MHz, switch selectable.
Channel 0	:	Internal 100 KHz or external clock (10 MHz max). The selection is controlled by the Timer/Counter Enable Register (BASE+10).

Pacer output : 0.00023 Hz (71 minutes/pulse) to 2.5 MHz.

1.2.6. Interrupt Channel

Level : IRQ 2 to 7, software selectable.

Enable : Via INTE bit of Control Register (BASE+9).

1.2.7. DMA Channel

Level : 1 or 3, jumper selectable.

Enable : Via DMAE bit of Control Register (BASE+9).

1.2.8. General

Power consumption :

+5 V	:	180 mA typical, 500 mA max.
+12V	:	140mAtypical, 200mAmax.
-12V	:	14 mA typical, 20 mA max.

I/O connector : 20 pin post headers for I/O connection. Adapter available to convert to 37 pin D-type connector

I/O base : Requires 16 consecutive address locations. Base address definable by the DIP switch SW3 for line A9-A4. (Factory setting is Hex 300).

Operating Temp : 0 to +50 °C.

Storage Temp : -20 to +65 °C.

CHAPTER 2. INSTALLATION

2.1. Initial Inspection

Inside the shipping container, you should find this operating manual and the PCL-818H card. The PCL-818H was carefully inspected both mechanically and electrically before shipment. It should be free of marks and scratches and in perfect mechanical and electrical order on receipt.

When unpacking, check the unit for signs of shipping damage (damaged box, scratches, dents, etc). If there is damage to the unit or if it fails to meet specifications, notify our service department or your local sales representative immediately. Also, call the carrier immediately and retain the shipping carton and packing material for inspection by the carrier. We will make arrangements to repair or replace the unit.

Remove the PCL-818H interface card from its protective packaging by grasping the rear metal panel. Keep the anti-vibration package. Whenever you remove the card from a PC expansion slot, please store the card in this package for protection.

Discharge any static electricity by touching the back of the system unit before you handle the board. You should avoid contact with materials that create static electricity such as plastic, vinyl, and styrofoam. The board should be handled only by the edges to avoid static electric discharge which could damage the integrated circuits on the PCL-818H.

2.2. Switch and Jumper Settings

The PCL-818 was designed with ease-of-use as a primary design concept. There are two functional switches and five jumper settings on the PCL-8l8H card, and the use of these switches and jumpers is discussed below. You may want to refer to Appendix B for the physical location of each switch and jumper.

2.2.1. Base Address Selection

- **Switch name: SW1**

The operation of the PCL-818H is controlled through the input and output ports. These ports are addressed using the I/O port address space. Appendix C provides a PC I/O port address map to help you locate appropriate addresses for different devices.

The I/O port base address for the PCL-818H is selectable via a 6 position DIP switch. The PCL-818H requires 16 consecutive address locations in I/O space. Valid base addresses are from Hex 000 to Hex 3F0. However, some of these addresses may be being used for other devices already. Your PCL-818H base address switch setting is set to Hex 300 in the factory. If you need to adjust it to some other address range, the switch settings for various base addresses are illustrated as below:

I/O Address Range (hex)	Switch Position					
	1	2	3	4	5	6
	A9	A8	A7	A6	A5	A4
000 - 00F	0	0	0	0	0	0
010 - 01F	0	0	0	0	0	1
.						
.						
200 - 20F	1	0	0	0	0	0
210 - 21F	1	0	0	0	0	1
.						
.						
300 - 30F *	1	1	0	0	0	0
.						
.						
3F0 - 3FF	1	1	1	1	1	1

Note :

- 0 = on, 1 = off
- A4...A9 correspond to the PC bus address lines.
- * means factory setting.

2.2.2. Channel Configuration

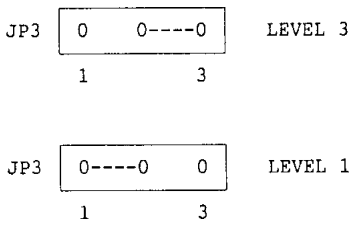
- **Switch name: SW2**

The PCL-8l8H offers 16 single-ended or 8 differential analog input channels. Slide switch SW2 controls the selection of the analog input configuration. Slide the switch to the left-hand position marked 'DIFF' for 8 differential inputs, or move the switch to the right-hand position marked 'S/E' for 16 single-ended inputs. The factory setting is for 'DIFF'.

2.2.3. DMA Channel Selection

- **Jumper name: JP3**

The PCL-818H provides a DMA data transfer capability. The selection of DMA level 1 or level 3 is controlled by this jumper. To use DMA level i, set jumper JP3 to the left-hand position marked '1'. Set the jumper to the right-hand position marked '3' for DMA level 3. The factory setting is for DMA level 3.



2.2.4. Timer Clock Selection

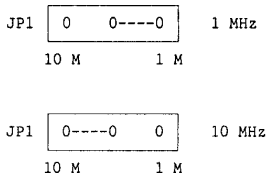
- **Jumper name: JP1**

The PCL-818H offers two input clock frequencies, 10 MHz and 1 MHz, for the 8254 programmable timer/counter to generate programmable pulses to trigger the A/D. After determining your A/D sampling rate and programming factors, set jumper JP1 to the left-hand position for 10 MHz, or to the right-hand

position for 1 MHz according to your requirements. The pacer rate to A/D is calculated as:

Pacer rate = Fclk /(Div1 * Div2)

where Fclk is 1 MHz or 10 MHz determined by the jumper JP1. Divl, Div2 are the dividers set in counter 1 and counter 2 respectively.

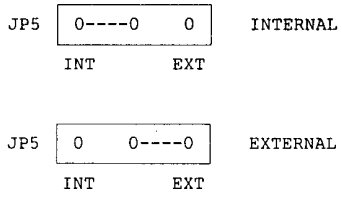


The factory setting is for 1MHz.

2.2.5. D/A Reference Voltage Selection

- **Jumper name: JP5**

The PCL-818H provides a jumper to select the reference voltage source of the D/A converters. Select either the internal reference or an external user-supplied reference with JP5.



When a jumper is inserted in the 'INT' position of JP5, the reference voltage input of the D/A channel is connected to an on-board reference. This reference

can be selected by JP4 to be either -5V or -10 V. In this condition, the D/A channel has an output range of 0 V to +5 V, or 0 V to +10V. When the jumper is inserted in position 'EXT' of JP5, the reference input of the D/A channel is routed to connector CN4 pin 1. Any voltage between -10 V and +10V can be applied to this pin to function as the external reference.

When an external reference is used and the voltage is V_{ref}, the D/A channel can be programmed to output from 0 V to $-V_{ref}$. The reference input can be either DC or AC (<100 KHz). In this manner, the D/A converter can be used as a programmable attenuator, the attenuation factor between reference input and analog output being:

Attenuation Factor = G / 4095

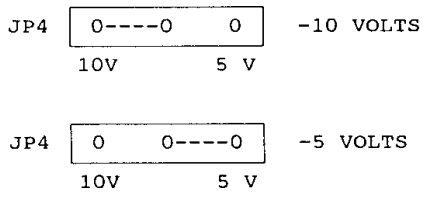
where G is the data written to the D/A registers and the value is between 0 and 4095. For example, if the data G is set to 2048, then the attenuation factor is 0.5, and a sine wave of 5 V amplitude applied to the reference input will generate a sine wave of 5 V amplitude on the analog output.

The factory setting for the D/A channel is for the internal reference .

2.2.6. Internal Voltage Reference Selection

- **Jumper name :JP4**

If JP5 is set to select the internal reference voltage, the PCL-818H provides a choice of two DC internal reference voltage sources: -5 V and -10 V. The selection is made with JP4. When the jumper is set to the left-hand position, -10 V is selected; setting the jumper to the right-hand position selects -5 V.



The factory setting is for -5 V.

2.2.7. TRIG0 and GATE0 Selection

- **Jumper name: JP2**

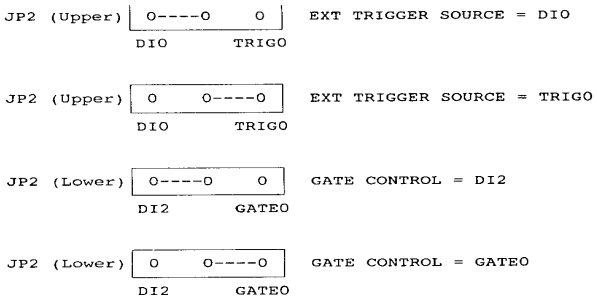
JP2 is reserved for TRIG0 and GATE0 selection. The various configurations are shown below:

Upper Jumper :

0 - Select external trigger. The trigger source is DI0
TRIG0 - Select external trigger. The trigger source is TRIG0

Lower Jumper :

2 - Select 8254 Counter 0. Gate is controlled by DI2.
GATE0 - Select 8254 Counter 0. Gate is controlled by **GATE0**



It is recommended that JP2 be set normally to positions DI0 and DI2 (both jumpers in the left-hand position), since this setting is required by the software driver. This setting has the same effect as that achieved by SW6 positions 7 and 8 on the PCL-718 card. The factory setting is for DI0 and DI2.

2.3. Connector Pin Assignment

The PCL-818H is equipped with two 20-pin insulation displacement (mass termination) connectors accessible from the rear panel, and two other onboard 20-piI1 insulation displacement connectors. All of these connectors can terminate the same type flat cables, or they may be used with 37-pin D-type connectors through our PCLK-1050 industrial wiring kit. Please refer to Appendix B for the location of each connector.

The following diagrams list the pin assignments of each connector:

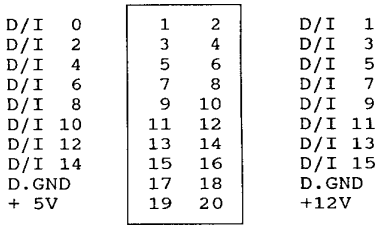
Legend:

A/D S	-	Analog input (single-ended)
A/D H	-	Analog input high (differential)
A/D L	-	Analog input low (differential)
A.GND	-	Analog ground
DIA	-	Analog output
D/O	-	Digital output
D/I	-	Digital input
D.GND	-	Digital and power supply ground
CLK	-	Clock input for the 8254
GATE	-	Gate input for the 8254
OUT	-	Signal output of the 8254
VREF	-	Voltage reference
REFIN	-	External voltage reference input

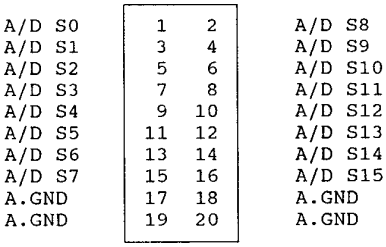
- CONNECTOR 1 (CN1) - Digital Output

D/O 0	1	2	D/O 1
D/O 2	3	4	D/O 3
D/O 4	5	6	D/O 5
D/O 6	7	8	D/O 7
D/O 8	9	10	D/O 9
D/O 10	11	12	D/O 11
D/O 12	13	14	D/O 13
D/O 14	15	16	D/O 15
D.GND	17	18	D.GND
+ 5V	19	20	+12V

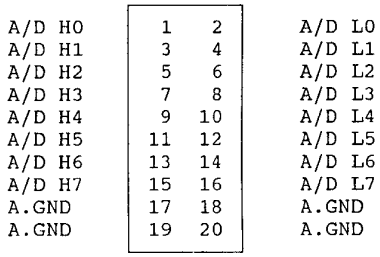
- CONNECTOR 2 (CN2) - Digital Input



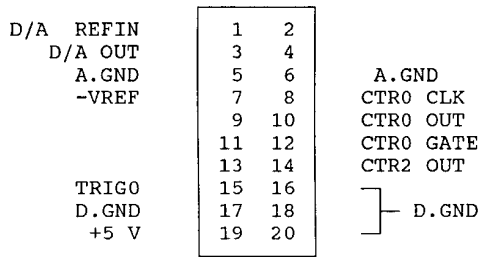
- CONNECTOR 3 (CN3) - Analog Input (Single-ended channels)



- CONNECTOR 3 (CN3) - Analog Input (Differential channels)



- **CONNECTOR** 4 (CN4) - Analog Output/Counter



2.4. Hardware Installation

```
************************ WARNING ***************************
**  TURN OFF your PC power supply whenever installing   **
**  or removing the PCL-818H or connecting and discon-  **
**  necting cables.                                     **
************************************************************
```

Installing the card in your computer:

1. Turn the computer off. Turn the power off to any peripheral devices (such as printers and monitors).

2. Disconnect the power cord and any other cables from the back of the computer. Turn the system unit so the back of the unit faces you.

3. Remove the system unit cover (see your User's Guide for your computer if necessary).

4. Locate the expansion slots at the rear of the unit and choose any unused slot.

5. Remove the screw that secures the expansion slot cover to the system unit (Save the screw to secure the interface card retaining bracket).

6. Carefully grasp the upper edge of the PCL-818H card. Align the hole in the retaining bracket with the hole on top of the expansion slot, and align the gold striped edge connector with the expansion slot socket. Press the board firmly into the socket.

7. Replace the screw in the expansion slot retaining bracket.

8. Attach necessary accessories (20 pin flat cable or connector adapter, etc.) to the interface card based on your application requirements.

9. Replace the system unit cover. Connect the cables you removed in step 2. Turn the computer power on.

Hardware installation is now complete. Proceed to install the software driver.

2.5. Software Disk

A floppy disk containing utility software is included with each PCL-818H to minimize your application programming works and support the PCL-8l8H calibration. The utility programs include:

1. A comprehensive I/O driver for A/D, D/A, Digital I/O and Counter applications. This driver allows you use standard functions, written in common programming languages, to operate the PCL-818H, without going into detailed register control. Languages supported by the software driver include BASICA, GWBASICI QUICKBASIC, Microsoft C/C + + and PASCAL, Turbo C/C + +, Borland C/C + + and Turbo PASCAL. Please refer to the Software Drivers User's Manual for more information.

2. Demonstration programs.

3. Calibration program.

4. Test program.

It is strongly recommended that you make a working copy from the master disk and save the master disk in a safe place. You may use the DOS COPY or DISKCOPY commands to copy the disk files to another floppy disk, or use the COPY command to copy the files to a hard disk.

CHAPTER 3. SIGNAL CONNECTION

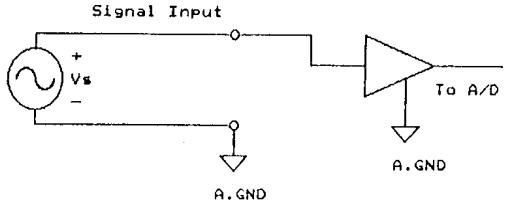
Correct signal connection is one of the most important factors to observe if your application is to send and receive data with accuracy. Good signal connections could avoid a lot of unnecessary damage to your valuable personal computer and other hardware devices. This chapter provides some useful information on signal connections in different types of data acquisition applications.

3.1. Analog Input Connection

The PCL-818H supports configurations of either 16 single-ended or 8 differential analog inputs. Input channel configuration is selected by means of slide switch (SW2) on the card. The major difference between single-ended and differential input connections is the number of signal wires per input channel.

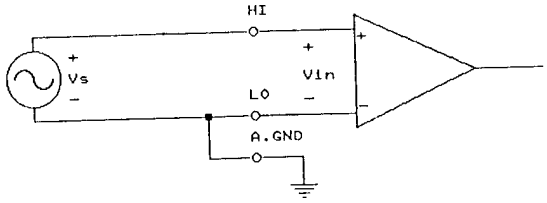
3.1.1. Single Ended Channel Connection

The single-ended configuration has only one signal wire per channel. The voltage to be measured is the voltage on this wire referenced to the common ground. A signal source without a local ground is called a "floating" source. It is fairly simple to connect a single ended channel to a floating signal source. A standard wiring diagram looks like this:



3.1.2. Differential Channel Connection

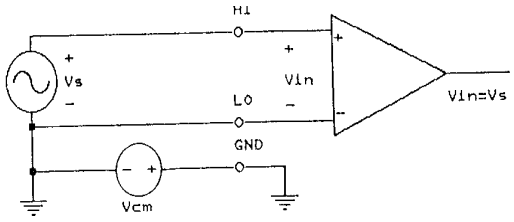
The differential input configuration uses two signal wires per channel. The differential input responds only to the voltage difference between these two wires, the HI and LOW. If the signal source has no connection to ground, it is called "floating" source. A connection must exist between Low and Ground to define a common reference point for floating signal sources. To measure a floating: source, the input channel should be connected as shown below:



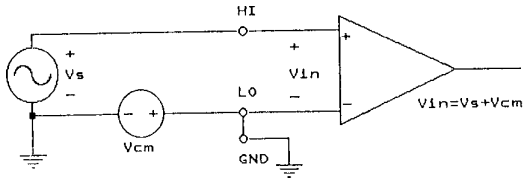
If the signal source has one side connected to a local ground, the signal source ground and the PCL-818H ground will not be at exactly the same voltage as they are connected through the ground return of the equipment and building wiring. The difference between the ground voltages forms a common-mode voltage.

To avoid the ground loop noise effect caused by common-mode voltages, the signal ground should be connected to the Low input. The Low input should not be connected to the PCL-818H ground directly. For better grounding in some cases, a wire connection between the PCL-8l8H ground and signal source ground may be necessary. The following two diagrams explain the correct and incorrect connections of a differential input with local ground:

Correct connection:



Incorrect connection:



3.2. Expanding Analog Inputs

User may expand any or all of the PCL-818H A/D input channels through sub-multiplexers. PCLD-789 Amplifier and Multiplexer Daughter Boards in the PC-LabCard series are specifically designed for multiplexing application. Each PCLD-789 can multiplex 16 differential inputs to one A/D input channel. Up to eight PCLD-789s can be cascaded to one PCL-818H, providing a total of 128 channels. Complete operation information for using the PCL-818H with the PCLD-789 is covered in the PCLD-789 user's manual.

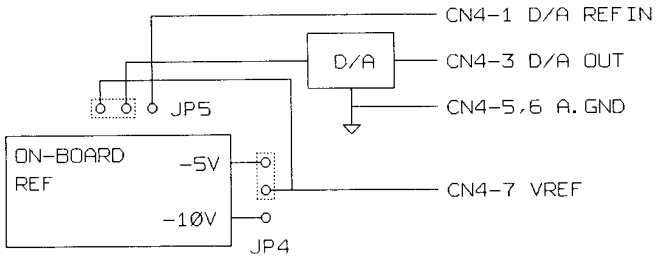
The PCLD-774 analog expansion board is designed to accommodate multiple external signal-conditioning daughterboards, such as PCLD-779 and PCLD-789. Featuring five sets of on-board 20-pin header connectors, the PCLD-774 introduces a new star-type architecture that allows cascading of multiple signal-conditioning boards. The signal-attenuation and current-loading problems of normal cascading are solved by this unique arrangement.

For information on any of these products, please contact your local PC-LabCard sales representative.

3.3. Analog Output Connection

The PCL-818H provides one D/A output channel. Users may use the internal precision -5 V (-10 V) reference to generate 0 to +5 V (+10V) D/A output range. Users may create other D/A output ranges through the use of an external reference. The maximum reference input voltage is ±10 V, and maximum

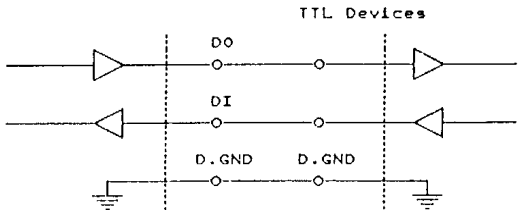
output scaling is ±10 V. The PCL-818H connector CN2 is used for D/A signals. Important D/A signal connections such as input reference, D/A outputs and analog ground are shown below. The loading current of D/A outputs should not exceed 5 mA.



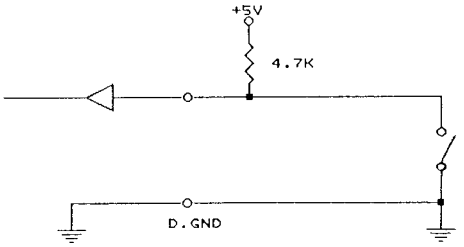
D/A CONVERTER SIGNAL CONNECTIONS

3.4. Digital Signal Connection

The PCL-818H has 16 digital input and 16 digital output channels. The digital I/O levels are TTL compatible. To transmit or receive digital signals to or from other TTL devices, the connections are as shown:



To receive an OPEN/SHORT signal from a switch or relay, a pull up resistor must be added to ensure that the input is held at a high level when the contacts are open.



CHAPTER 4. REGISTER STRUCTURE AND FORMAT

The PCL-818H requires 16 consecutive addresses in I/O space. The most important factor in programming the PCL-818H is understanding the meaning of the 16 registers addressable from the selected I/O port base address. A summary map of the function of each address and the data format of each register are included in the following sections.

4.1. I/O Port Address Map

The following table shows the relative location of each register and driver as to its base address and usage.

Location	Read	Write
BASE+0	A/D low byte & channel	Software A/D rigger
BASE+1	A/D high byte	A/D range control
BASE+2	MUX scan channel	MUX scan channel & range control pointer
BASE+3	D/I low byte (DI0-7)	D/O low byte (D00-7)
BASE+4	N/A	D/A 0 low byte
BASE+5	N/A	D/A 0 high byte
BASE+6	N/A	N/A
BASE+7	N/A	N/A
BASE+8	Status	Clear interrupt request
BASE+9	Control	Control
BASE+10	N/A	Counter enable
BASE+11	D/I high byte (DI8-15)	D/O high byte (DO8-15)
BASE+12	Counter 0	Counter 0
BASE+13	Counter 1	Counter 1
BASE+14	Counter 2	Counter 2
BASE+15	N/A	Counter control

4.2. A/D Data Registers

The A/D data registers are read-only registers using addresses BASE+0 and BASE+1. The A/D conversion 12 bit data is in register BASE+1 bit 7 to bit 0, and the register BASES+0 bit 7 to bit 4. The A/D channel number from which the conversion data is derived is available at register BASE+0, bit 3 to bit 0.

Data Format:

1. A/D low byte and channel number.

BASE+0	D7	D6	D5	D4	D3	D2	D1	D0
(read port)	AD3	AD2	AD1	AD0	C3	C2	C1	C0

2. A/D high byte.

BASE+1	D7	D6	D5	D4	D3	D2	D1	D0
(read port)	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

Legend:

AD11 to AD0 - Analog to digital data. AD0 is the least significant bit (LSB), and ADI1 is the most significant bit (MSB) of the A/D data.
C3 to C0 - A/D channel number from which the data is derived. C3 is the MSB and C0 is the LSB.

4.3. Software A/D Trigger

The A/D converter can be triggered by 3 sources: from software, on-board pacer or from external pulses. The selection of trigger sources is controlled by the BASE+9 Control Register bit 1 and bit 0. If the trigger source is selected to be software, a writing act to the register BASE+0 with any value will trigger an A/D conversion.

4.4. A/D Range Control

The A/D range is controlled by the Range Codes stored in an on-board RAM, and each channel of A/D has its own individual input range. The range code of each channel (total of 16 channels) is written to the on-board RAM through register BASE + l by software, and the related channel is the current channel of the MUX which is controlled by writing register BASE+2.

BASE+1	D7	D6	D5	D4	D3	D2	D1	D0
(write port)	N/A	N/A	N/A	N/A	G3	G2	G1	G0

Range Code				Unipolar/Bipolar	Input Range
G3	G2	G1	G0		
0	0	0	0	B	± 5V
0	0	0	1	B	± 2.5V
0	0	1	0	B	± 1.25V
0	1	0	0	B	± 0.625V
0	1	0	0	U	0 - 10V
0	1	0	1	U	0 - 5V
0	1	1	0	U	0 - 2.5V
0	1	1	1	U	0 - 1.25V
1	0	0	0	B	± 10V
1	0	0	1		Invalid
1	0	1	0		Invalid
1	0	1	1		Invalid
1	1	0	0		Invalid
1	1	0	1		Invalid
1	1	1	0		Invalid
1	1	1	1		Invaild

Note: Unipolar and Bipolar inputs cannot be mixed in Auto Channel Scan Mode. Inputs must be either all bipolar or all unipolar.

4.5. MUX Scan Register

The MUX scan register is a read/write register using address BASE+2. The high nibble provides the stop scan channel number and the low nibble provides the start scan channel number. The MUX is initialized automatically to the start channel when writing to this register. Each trigger of AID will set the MUX to the next channel. For continuous triggering, the MUX will scan between the start channel and the stop channel sequentially. For example, if the start channel is 3 and the stop channel is 7, then the scan sequence is 3, 4, 5, 6, 7, 3, 4, 5, 6, 7, 3, 4...

Data Format:

BASE+2 (write port)	D7	D6	D5	D4	D3	D2	D1	D0
Stop scan & start scan	CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Legend:

CH3 to CH0 - Stop scan channel number.

CL3 to CL0 - Start scan channel number.

The MUX scan register low nibble, CL3 to CL0, also acts as a pointer when programming the A/D input range. When the MUX is set to channel N, the range code written to the register BASE+1 is for channel N.

Example:

Set channel 5 to ±0.625 V input range with BASIC:

```
200  OUT BASE+2, 5    'SET POINTER TO CH.5
210  OUT BASE+1, 3    'RANGE CODE=3 FOR ±0.625 V
```

Since every time the pointer is set for range setting, the MUX start/stop channel setting is also changed, do not forget to set the MUX start/stop channel to correct numbers after the range setting.

4.6. Digital I/O Registers

The PCL-818H offers 16 digital input channels and 16 digital output channels. These I/O channels use the input and output ports at address BASE+3 and BASE+11. The data format of each port is as shown below:

Data Format:

BASE+3 (read port)	D7	D6	D5	D4	D3	D2	D1	D0
D/I low byte	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

BASE+3 (write port)	D7	D6	D5	D4	D3	D2	D1	D0
D/O low byte	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

BASE+11 (read port)	D7	D6	D5	D4	D3	D2	D1	D0
D/I high byte	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

BASE+11 (write port)	D7	D6	D5	D4	D3	D2	D1	D0
D/O high byte	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8

4.7. D/A Output Registers

The D/A output registers are write only registers using address BASE+4, BASE +5.

Data Format:

BASE+4	D7	D6	D5	D4	D3	D2	D1	D0
D/AO low byte	DA3	DA2	DA1	DA0	X	X	X	X

BASE+5	D7	D6	D5	D4	D3	D2	D1	D0
D/AO high byte	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4

Legend:

DA11 to DA0 - Digital to analog data. DA0 is the least significant bit (LSB) and DAI1 is the most significant bit (MSB) of the D/A data.

4.8. A/D Status Register

The A/D status register is a read-only register using address BASES+8. This register provides information on the configuration and operation of the A/D in the PCL-818H. A write operation to this I/O port with any data value clears the INT bit of this register and the other data bits are not changed.

Data Format:

BASE+8	D7	D6	D5	D4	D3	D2	D1	D0
A/D status	EOC	UNI	MUX	INT	CN3	CN2	CN1	CN0

Legend:

EOC - End of Conversion.

EOC = 0, means the A/D converter is in the idle state and is ready for the next conversion. The previous conversion data is available in the A/D data registers.

EOC = 1, means the A/D converter is busy and implies that the A/D conversion is proceeding.

UNI - Unipolar/Bipolar mode indicator.

U/B = 0 Bipolar mode.

U/B = 1 Unipolar mode.

MUX - Single-ended / Differential mode indicator.

MUX = 0 8 differential channels mode.

MUX = 1 16 single-ended channels mode.

INT –Data valid.

INT = 0, No A/D conversion completed since last clear of INT bit. No A/D conversion data is valid.

INT = 1, A/D conversion is completed and conversion data is ready. If the INTE bit of the control register (BASE+9) is set, an interrupt signal will be sent to the PC bus through interrupt level IRQn where n is specified by bits I2, Il and I0 of the control register. The A/D status register is read-only. However, a writing act to this register with any value will clear this INT bit.

CN3 to CN0 - Next channel to be converted

When EOC = 0, these status bits contain the channel number of the next channel to be converted.

Remarks:

If the user uses the on-board pacer or external pulses as the A/D trigger source, the INT bit, not EOC bit, should be checked by the software before reading the conversion data. When EOC = 0, the situation can be either (a) conversion is completed or (b) no conversion has been started. Therefore, the software should wait for the signal INT=I before reading the conversion data, and should then clear the INT bit by writing any value to the A/D status register BASE+8.

4.9. Control Register

The PCL-818H control register is a read/write register using address BASE+9. This register provides information on the operating modes of the PCL-818H.

Data Format:

BASE+9	D7	D6	D5	D4	D3	D2	D1	D0
Control	INTE	I2	I1	I0	X	DMAE	ST1	ST0

Legend:

INTE - Disable/Enable PCL-818H generated interrupts.

INTE = 0, disables the generation of interrupts. No interrupt signal can be sent to the PC bus.

INTE = 1 and DMAE = 0, enables the generation of an interrupt when an A/D conversion is completed. This is for interrupt driven data transfer.

INTE = 1 and DMAE = 1 enables the generation of an interrupt when a TIC (terminal count) signal is received from DMA controller, indicating the completion of a DMA transfer. This is for DMA data transfer and the transfer can be stopped by the interrupt caused by the T/C signal.

I2 to I0 - Interrupt level selection.

INL2	INL1	INL0	Interrupt Level
0	0	0	N/A
0	0	1	N/A
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

Do not use a level which is being used by other I/O devices.

DMAE - Disable/Enable PCL-818H DMA transfers.

DMAE = 0, disables the DMA transfer.
DMAE = 1, enables the DMA transfer. Each A/D conversion initiates two DMA request signals sequentially to cause the 8237 DMA controller to transfer two bytes of the conversion data from the PCL-818H to memory.

The 8237 DMA controller and the DMA page register on the PC system board must be programmed accordingly, before the DMA bit of this control register is set true.

ST1 to ST0 - Source of trigger.

ST1	ST0	Source of Trigger
0	X	Software trigger
1	0	External trigger
1	1	Pacer trigger

4.10. Timer/Counter Enable Register

The Timer/Counter register is a write register using 2 bits at address BASE+10.

Data Format:

BASE+10	D7	D6	D5	D4	D3	D2	D1	D0
	X	X	X	X	X	X	TC1	TC0

Legend:

TC0 - Pacer Disable/Enable.

TC0 = 0, peer enabled.
TC0 = 1, pacer controlled by TRIG0. This holds off trigger pulses to the A/D from the pacer until TRIG0 is taken high.

TC1 - Counter 0 input source mode.

TC1 = 0, means Counter 0 is configured to accept external clock pulses.
TCI = 1, means Counter 0 is internally connected to a 100 KHz clock source.

4.11. Programmable Timer/Counter Registers

The four registers located at addresses BASE+ 12, BASE + 13, BASE+ 14 and BASE+15 are used for the Intel 8254 programmable timer/counter. Please refer to Chapter 8 or 8254 product literature for detailed application information .

CHAPTER 5. A/D CONVERSION

This chapter provides a complete explanation of how to use the PCL-818H A/D conversion functions. It covers A/D data format, input range selection, status register, MUX scan setting, trigger modes and data transfer in the first five sections. The last section gives step by step implementation guidelines on A/D operations.

5.1. A/D Data Format and Status Register

Since the PCL-818H uses 12 bit A/D conversions, an 8 bit register is not enough to accommodate all 12 bits of data. Therefore, A/D data is stored in two registers located at addresses BASE+0 and BASE+1.

The A/D low byte data are in positions D4 (AD0) through D7 (AD3) of BASE+0, and high byte data are in positions D0 (AD4) through D7 (AD11) of BASE+1. The least significant bit is AD0 and the most significant bit is AD11. The A/D channel number from which the conversion data is derived is available at BASE+0 position D0 (C0) to D3 (C3).

The data formats of the A/D data registers are as follows:

BASE+0	D7	D6	D5	D4	D3	D2	D1	D0
A/D low byte and channel	AD3	AD2	AD1	AD0	C3	C2	C1	C0

BASE+1	D7	D6	D5	D4	D3	D2	D1	D0
A/D high byte	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

Information on the configuration and operation of the A/D in the PCL-818H is available at the A/D status register, which is a read-only register using address BASE + 8.

The data format of the A/D status register is:

BASE+8	D7	D6	D5	D4	D3	D2	D1	D0
A/D status	EOC	UNI	MUX	INT	CN3	CN2	CN1	CN0

The information contained in this register includes the end of conversion status, unipolar/bipolar input, single-ended/differential configuration, interrupt status and next to be converted channel number. Please refer to Section 4.8. (A/D Status Register), for more information.

5.2. Input Range Selection

The input range is programmable, and each input channel has its own range which is defined by the range code stored in the on-board RAM. Please refer to Sections 4.4. and 4.5. for information concerning remote range control.

5.3. MUX Setting

The PCL-818H offers 16 single-ended or 8 differential analog input channels. The user should adjust the channel configuration slide switch (SW2) before setting the multiplexer scan range. The high and low limits of the scan range are specified in the MUX scan register. The MUX scan register is a read/write register using address BASE+2. Positions D0 through D3 are used for the start scan channel number, and positions D4 through D7 are used for stop scan channel number. When using the 8 channel differential input mode, the bits CH3 and CL3 must be zero.

The data format of the MUX scan register is:

BASE+2	D7	D6	D5	D4	D3	D2	D1	D0
MUX scan	CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

If only one A/D input channel is required, the high and low scan limits must be set to equal. If a range of input channels is specified, the A/D conversion is performed from the start scan channel and incremented by one channel at a time until the stop scan channel reached. This looping is continued until the number f conversions specified is completed. Please note that the MUX channel is set to start channel automatically when writing to this register.

The user may specify the channel setting by writing directly to the MUX scan I/O port. To program the range code of each input channel, the MUX scan register acts as a pointer. After setting the range codes, the correct start/stop channel must be set to this register to ensure proper operation.

5.4. Trigger Mode

The PCL-818H A/D conversions can be triggered in any one of following three ways: software trigger, on-board programmable pacer trigger and external pulse trigger.

1. The software trigger is controlled by a software command issued by the application program. A writing act to register BASE+0 with any data generates a trigger to the A/D converter. This trigger mode is not normally used in high speed A/D applications due to the limitations of application program execution time.

2. The PCL-818H uses the Intel 8254 programmable interval timer/ counter to generate timing related signals. Counters 1 and 2 of the Intel 8254 are configured as a pacer to offer A/D converter trigger pulses with precise periods in pacer trigger mode. The pacer output of the PCL-818H is between 2.5 MHz and 71 minutes per pulse. Chapter 8 covers the details of the Intel 8254 timer/counter. The pacer trigger mode is ideal for interrupt and DMA data transfer which is normally used in A/D applications requiring higher conversion speeds.

3. The PCL-818H external trigger signal is named TRIG0 (connector CN2 pin 15). This type of trigger mode is used mostly in A/D applications requiring A/D conversions not periodically, but conditionally; e.g., measuring a voltage when a limit switch closes. The A/D conversions start at the rising edge of external trigger pulses.

5.5. A/D Data Transfer

There are three possible ways to perform A/D data transfer: by program control, interrupt routine or DMA.

1. The program control data transfer uses the polling concept. After the A/D converter has been triggered, the application program checks the INT bit (data valid) of the A/D status register. When the INT bit is detected as a 1, the converted data is moved from the A/D data register to the computer memory by application program. Remember to clear the INT bit by writing to register BASE+8 with any value after the AID data is retrieved.

   When using the software trigger, since the timing of A/D conversion is controlled by program, either the INT or EOC bits of the A/D status register can be checked for data validity. It is easier to use the EOC bit, since the necessity of clearing the INT bit can be avoided.

3. In interrupt routine transfer, data is transferred from A/D data register to a previously defined memory segment by the interrupt routine handler. At the end of each conversion, the EOC signal generates an interrupt which enables the interrupt handler routine to perform the transfer. The interrupt control bit and interrupt level selection bits in the PCL-818H control register (BASE+9) must be specified before the use of the interrupt routine. A write action to the AID status register address (BASE+8) resets the PCL-818H interrupt request and re-enables the PCL-818H interrupt.

3. Direct memory access (DMA) transfer moves the A/D data from the PCL-81811 hardware device to the PC system memory without operation of the system CPU. DMA is very useful in high speed data transfer, but it is complicated to operate. The DMA level selection facility (JP3) and the DMA enable bit in the PCL-818H control register as well as the 8237 MA controller registers, must be set up before the DMA operation. It is recommended to use the PCL-818 driver to perform DMA operation. For more information regarding the 8237 DMA controller and the PCL-818H DMA operations, please read Chapter 9.

5.6. flow to Make an A/D Conversion

You may perform A/D operations by means of a program writing all I/O port instructions directly, or by means of a program utilizing the PCL-818H driver. It is suggested that you make use of the driver functions in your program. This will make your programming job easier, and enhance the program performance. See Software Drivers User's Manual for more information.

To perform software trigger and program control data transfer without the PCL- 818 driver:

Step 1 : Set the input range of each AID channel.

Step 2 : Set input channel by specifying the MUX scan range.

Step 3 : Trigger A/D by writing to the A/D low byte register (BASE+0) with any value.

Step 4 : Wait for the end of conversion by reading the A/D status register (BASE+8) INT bit.

Step 5 : Read data from A/D converter by reading the A/D data registers (BASE+0 and BASE+1).

Step 6 : Data conversion by converting the binary A/D data to an integer.

CHAPTER 6. D/A CONVERSION

6.1. General Information

The PCL-818H provides one D/A channel which uses two double buffered 12 bit multiplying D/A converters. The D/A registers are write registers using address BASE+4, BASE+5. DA0 is the least significant bit (LSB) and DA11 is the most significant bit (MSB) of the D/A data. A summary of each register's data format follows:

BASE+4	D7	D6	D5	D4	D3	D2	D1	D0
D/A0 low byte	DA3	DA2	DA1	DA0	X	X	X	X

BASE+5	D7	D6	D5	D4	D3	D2	D1	D0
D/A0 high byte	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4

When writing to the D/A channels, please note that the low byte should be written first. It is temporarily held by a register in the D/A and not released to the output. After the high byte is written, the low byte and high byte are added and passed to the D/A converter. This double buffering process protects the D/A data integrity through a single step update.

The PCL-818H provides a precision fixed internal -5 V or -10 V reference, selectable by means of Jumper JP4 (See Section 2.2.8). This reference voltage is available at connector CN2 pin 7. If this voltage is used as the D/A reference input, the D/A output range will be either 0 to +5 V or 0 to +10 V. Other external DC or AC sources may be used as the D/A reference input. In this case, the maximum reference input voltage is ±10V, and the maximum D/A output ranges will be 0 to +10V or 0 to -10V respectively.

Connector CN2 supports all D/A signal connections. The pin assignment of connector CN2 is described in Section 2.3.. Section 3.3 explains D/A signal connection with a wiring diagram.

6.2. D/A Applications

A variety of D/A operations can be supported by the PCL-818H; e.g., it is capable of functioning as a digital attenuator by input variable AC or DC references, or as a generator of arbitrary waveforms. In a similar way to that used for A/D programming, the D/A functions can be utilized in two ways: using either the PCL-818H driver functions in the application program or writing I/O instructions directly to the registers.

CHAPTER 7. DIGITAL INPUT AND OUTPUT

The PCL-8l8H provides 16 digital input channels and 16 digital output channels. These I/O channels use the input and output registers at address BASE+3 and BASE+11. A summary of each register's data format is listed below :

BASE+3 (read port)	D7	D6	D5	D4	D3	D2	D1	D0
D/I low byte	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

BASE+3 (write port)	D7	D6	D5	D4	D3	D2	D1	D0
D/I low byte	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

BASE+11 (read port)	D7	D6	D5	D4	D3	D2	D1	D0
D/I high byte	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8

BASE+11 (write port)	D7	D6	D5	D4	D3	D2	D1	D0
D/I high byte	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8

It is fairly straightforward to use the digital input and output functions of your PCL-818H. Section 3.4. offers some ideas about digital signal connections.

CHAPTER 8. PROGRANIIVIABLE TIMERICOUNTER

8.1. The Intel 8254

The PCL-818H uses the Intel 8254 programmable interval timer /counter version 2. The 8254 is a very popular timer/counter device consisting of three independent 16 bit down counters. Each counter has a clock input, control gate and an output. It can be programmed to have a count from 2 up to 65535.

The maximum input clock frequency is 10 MHz for Version 2 of the 8254. The PCL-818H provides 1 MHz and 10 MHz input frequencies from an on- board crystal oscillator. The timer clock jumper JP1 is used for clock input rate selection (See Section 2.2.6.).

Counters 1 and 2 are cascaded and operated in a fixed divider configuration. Counter 1 input is connected to the 1 MHz or 10 MHz clock frequency and the output of Counter 1 is connected to the input of Counter 2. The output of Counter 2 is internally configured to provide trigger pulses to the A/D converter, but it also available to the user on connector CN4 pin 14. As Counter 0 is not reserved by the PCL-818H for any internal use, the user may access Counter 0 through connector CN4. Please refer to the Section 2.3. for connector CN4 pin assignment.

8.2. Counter Read/Write and Control Registers

The 8254 programmable interval timer uses four registers at address BASE+12 BASE+l3, BASE+14 and BASE+15. The functions of each register are as follows:

BASE + 12	Counter 0 Read/Write
BASE + 13	Counter 1 Read/Write
BASE + 14	Counter 2 Read/Write
BASE + 15	Counter Control Word

Since the 8254 counter uses a 16 bit structure, each section of read/write data is split into the least significant byte (LSB) and the most significant byte (MSB). It is important to ensure that your read/write operations are in pairs and to keep rack of the byte order.

The data format of the control register is:

BASE+15	D7	D6	D5	D4	D3	D2	D1	D0
Control	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

Legend:

SC1 & SC0 - Select Counter.

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-back command

RW1 & RW0 - Select the Read/Write operation.

RW1	RW0	Operation
0	0	counter latch
0	1	Read/Write LSB
1	0	Read/Write MSB
1	1	Read/Write LSB first, then MSB

M2, M1 and M0 - Select the Operating Mode.

M2	M1	M0	Mode
0	0	0	0 interrupt is terminal count
0	0	1	1 programmable one shot
X	1	0	2 Rate generator
X	1	1	3 Square wave rate generator
1	0	0	4 Software triggered strobe
1	0	1	5 Hardware triggered strobe

BCD - Select Binary or BCD Counting.

BCD	Type
0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter

If the module is set to be binary, the count can be any number from 0 up to 65535. If the module is set to be BCD (binary coded decimal), the count can be set as any number from 0 to 9999.

If both SC1 and SC0 bit are set to i, the counter control register is in read-back command. The data format of the control register then becomes:

BASE+15	D7	D6	D5	D4	D3	D2	D1	D0
	1	1	CNT	STA	C2	C1	C0	X

Legend :

CNT = 0 Latch count of selected counter(s).

STA = 0 Latch status of selected counter(s).

C2, C1 and C0 - Select counter for a read-back operation.
C2 = 1 select Counter 2
C1 = 1 select Counter 1
C0 = 1 select Counter 0

If SC1 and SC0 are both set to 1 and STA is set to 0, the counter read/write register selected by C2 to C0 contains a return status byte. The data format of the counter read/write register then becomes:

BASE+12/13/14	D7	D6	D5	D4	D3	D2	D1	D0
	OUT	NC	RW1	RW0	M2	M1	M0	BCD

Legend:

OUT - Counter output current state
NC - Null count indicates when the last count written to the counter rgister has been loaded into the counting element.

The counter enable register located at address BASE+10 has a close relationship with the counter operation. Please refer to Section 4.10 for the data format of this 2 bit write only register. The TC0 bit controls the pacer enable/disable. If TC0 = 0, the pacer is enabled. If TC0 = 1, it disables the pacer and holds off trigger pulses to the A/D from the pacer until TRIG0 is taken high. The TCI bit controls Counter 0 input source. If TC1 = 0, Counter 0 is configured to accept external clock pulses. If TCI = 1, Counter 0 is internally connected to the 100 KHz clock source.

8.3. Counter Operating Modes

8.3.1. MODE 0 - Stop on Terminal Count

The output will be initially low after setting this mode of operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When the terminal count is reached, the output will go high and remain high until the selected counter is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached. Rewriting a counter register during counting generates the following results:

1. Write the first byte stops the current counting.

2. Write the second byte starts the new count.

8.3.2. MODE 1 - Programmable One-Shot

The output will go low on the count following the rising edge of the gate input. The output will go high on the terminal count. If a new count value is loaded while the output is low, it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse. The one-shot is retriggerable, thus the output will remain low for the full count after any rising edge at the gate input.

8.3.3. MODE 2 - Rate Generator

The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the counter register. If the counter register is reloaded between output pulses, the present period will not be affected, but the subsequent period will reflect the value. The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Therefore the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until the count register is loaded and the output can also be synchronized by software.

8.3.4. MODE 3 - Square Wave Generator

Similar to Mode 2, except that the output will remain high until one half of the count has been completed (for even numbers), and will go low for the other half of the count. This is accomplished by decreasing the counter by two on the falling edge of each clock pulse. When the counter reaches the terminal count, the state of the output is changed, the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the count by 2· After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by two until timeout, then the whole process is repeated. In this way, if the count is odd, the output will be high for (N+1)/2 counts and low for (N-1)/2 counts.

8.3.5. MODE 4 - Software Triggered Strobe

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, and will then go high again.

If the count register is reloaded during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

8.3.6. MODE 5 - Hardware Triggered Strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable.

8.4. Counter Operations

8.4.1. Read/Write Operation

For each counter, the type of read/write operation, operating mode and counter type all must be properly specified in the control byte, and the control byte must be written before the initial count is written.

Since the control byte register and all three counter read/write registers have separate addresses and each control byte specifies the counter it applies to (by SC1 & SC0), no instructions on the operating sequence are required. Any programming sequence following the 8254 convention is acceptable.

There are three types of counter operation: read/load LSB, read /load MSB and read /load LSB followed by MSB. It is important to ensure your read/write operations are in pairs and to keep track of the byte order.

8.4.2. Counter Read-Back Command

The 8254 counter read-back command allows users check the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter(s). The command is written into the control word register and has the format shown in Section 8.2.

The read-back command may be used to latch multiple counter output latches by setting the CNT bit = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched.

The read-back command can also be used to latch status information of selected counter(s) by setting STA bit = 0. Status must be latched to be read; the status of a counter is accessed by a read from that counter. The counter status format is shown in Section 8.2..

8.4.3. Counter Latch Operation

It is often desirable to read the value of a counter without disturbing the count in progress. Usually the method used is the counter latch command method which allows the user to read the latched count value of the selected counter.

The 8254 supports the counter latch operation in two ways. The first way is to set the RWI & RW0 to be (0,0) which latches the count of the selected counter in a 16 bit hold register. The second approach is by performing a latch operation under the read-back command by setting the SC1 & SC0 to be (1,1) and CNT = 0. This method has the advantage of operating several counters at the same time. A subsequent read operation on the selected counter will retrieve the held value.

8.5. Counter Applications

The 8254 programmable interval timer/counter on your PCL-818H interface card is a very useful device. In this section, two of the most popular usages of the 8254 timer/counter are introduced.

1. If you are using the A/D function of the PCL-818H, the 8254 can be programmed to serve as a pacer to generate A/D trigger pulses.

2. The Counter 0 of the 8254 is not committed to any internal use. Users may configure the Counter 0 to perform any 8254 supported function; e.g., a square wave generator.

CHAPTER 9. DIRECT MEMORY ACCESS OPERATION

Direct memory access (DMA) improves system performance by allowing external devices to transfer information directly to or from the system memory without operation of the system CPU. The PCL-818H is designed with A/D data DMA transfer capability. This feature significantly improves the system performance in high speed A/D applications.

9.1. Introduction to the 8237 DMA Controller

DMA is controlled by the 8237 DMA controller chip on the PC's system board. It has four prioritized direct memory access channels. Channel 0 is reserved by the PC system to perform dynamic RAM refresh; Channel 2 is always assigned to support floppy disk operations. Channel 3 is normally used by the hard disk operations. Channel 1 is not reserved for any internal operations and is available for the user's applications.

Each channel has two control signals associated with it. The DMA request signal (DRQ) triggers a DMA operation, and the DMA acknowledge signal (DACK) authorizes the DMA to start data transfer.

In addition to four DMA channels, the 8237 DMA chip has four operating modes (single, demand, block and cascade), and four control registers. These registers are:

1. Operation mode register (set operation mode).
2. Address register (specify memory segment starting address).
3. Word count register (specify the number of transfers).
4. Initialization register (enable and disable DMA channels).

Please note that all four registers must be properly set up before the DMA operation can be requested.

9.2. Using DMA Transfer with the PCL-818H

DMA transfer is a powerful but complicated operation. Different subjects regarding the DMA transfer have been covered in many chapters of this manual. The following is a summary of how to use DMA transfer with the PCL-818H.

1. On hardware configuration, check your PC DMA channel availability (level 1 or level 3) and set the PCL-818H jumper JP3 accordingly.

2. If you choose to use the PCL-818H driver to support the DMA transfer programming, see the Software Drivers User's Manual for more detailed information.

3. If you choose to conduct your own DMA operation, you need to have a solid understanding of the PC, 8237 DMA controller and the PCL-818H device. To complete a DMA transfer, make sure you have covered the following operations.

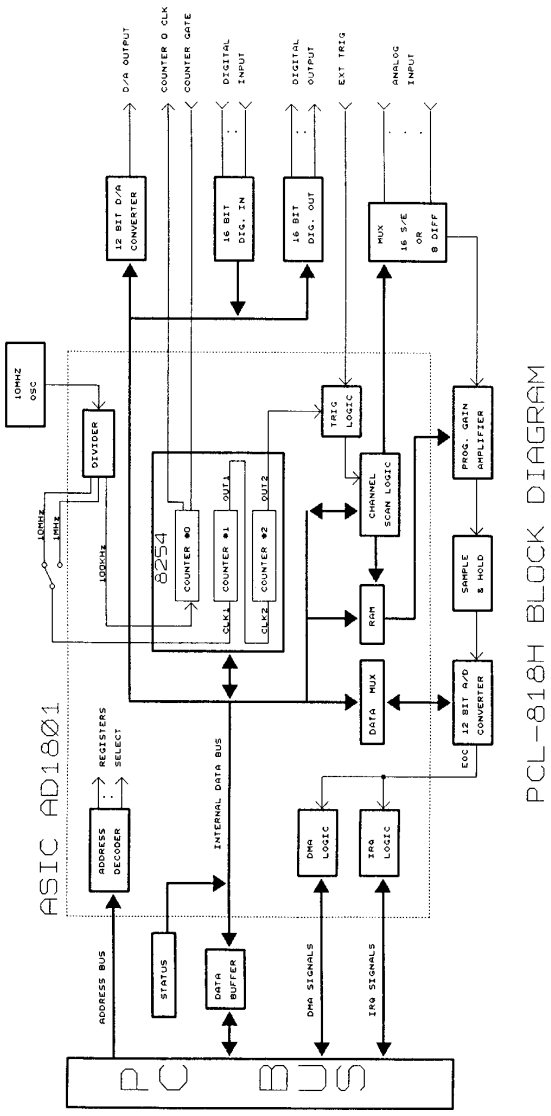
a. Initialize 8237 DMA controller register and page register.

b. Send DMA enable and trigger source data to the PCL-818H control register located at address BASE+9.

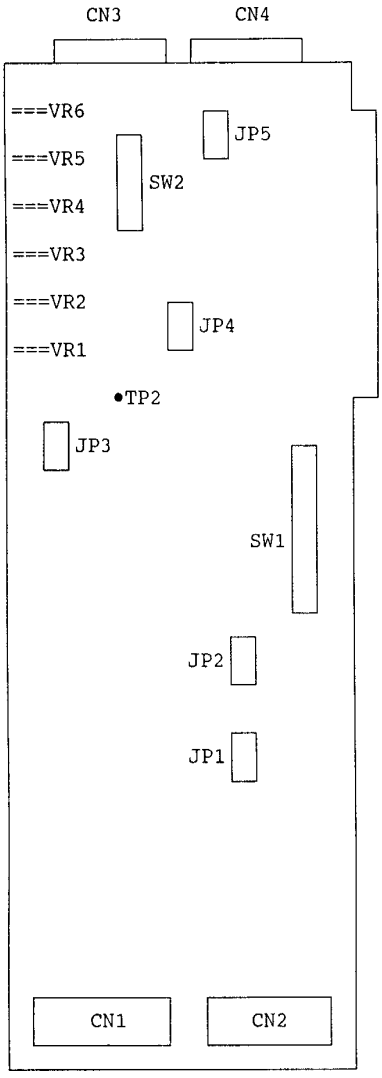
c. Set up external trigger pulse or pacer trigger rate.

d. Enable trigger source to start A/D conversion

APPENDIX A - BLOCK DIAGRAM



APPENDIX B - CONNECTOR, SWITCH & VR LOCATIONS



Legend:

CN1: Digital output
CN2: Digital input
CN3: Analog input
CN4: Analog/Counter out

SW1: Base address
SW2: Diff/Single-ended

JP1: 10 MHz/1 MHz time-base
JP2: TRIG0, GATE0 connection
JP3: DMA level
JP4: -5 V/-10 V reference
JP5: D/A reference select

VR1: Unipolar offset
VR2: A/D Full Scale
VR3: Bipolar offset
VR4: PGA offset
VR5: D/A full scale
VR6: D/A Offset

TP2: Test Point 2

APPENDIX C - PC I/O PORT ADDRESS MAP

I/O Address Range (hex)	Function
000 - 1FF	Base system
200	Reserved
201	Game control
202 - 277	Reserved
278 - 27F	LPT2: (2nd printer port)
280 - 2F7	Reserved
2F8 - 2FF	COM2:
300 - 377	Reserved
378 - 37F	LPT1: (1st printer port)
380 - 3AF	Reserved
3B0 - 3BF	Mono Display/Print adapter
3C0 - 3CF	Reserved
3D0 - 3DF	Color/Graphics
3E0 - 3EF	Reserved
3F0 - 3F7	Floppy disk drive
3F8 - 3FF	COM1:

APPENDIX D – CALIBRATION

In data acquisition and control applications, it is important to carry out regular calibration checks in order to maintain accuracy. A calibration program, CALB.EXE, is provided on the PCL-818H software disk to assist you in this task.

A 4 1/2 digit digital multimeter is required as the minimum equipment to perform a satisfactory calibration. In addition, a voltage calibrator or a stable, noise free D.C. voltage source which can be used in conjunction with the digital multimeter is required. A card extender, such as the PC-LabCard model PCL- 757 (ISA-Bus Switch/Extension Card) is a device which provides easy and safe access to the board during calibration, and will be a valuable tool for other functions as well.

Calibration is easily performed using the CALB.EXE program. This program will lead you through the calibration and set-up procedure with a variety of prompts and graphic displays, showing you all of the correct settings and adjustments. The explanatory material in this section is brief and is intended for use in conjunction with the calibration program.

D.1. VR Assignment

There are 6 variable resistors (VRs) on the PCL-8l8H to allow you to make accurate adjustments on all AID and D/A channels. The location of each VR is indicated in Appendix B (PCL-818H Connector, Switch and VR Locations). The function of each VR is listed below:

VR1 : Unipolar offset
VR2 : A/D Full scale adjustment
VR3 : Bipolar offset
VR4 : Programmable Gain Amplifier offset
VR5 : D/A full scale
VR6 : D/A offset

D.2. A/D Calibration

Regular and accurate calibration procedures will allow the user to achieve maximum possible accuracy. The calibration program (CALB. EXE) will lead you to go through the whole procedure for adjustment of A/D offset and gain. The basic steps are outlined as below:

1. Short the A/D input channel 0 to ground and measure the voltage at TP2. Adjust VR4 to 0V as close as possible.

2. Select bipolar input configuration. Connect a DC voltage source (D/A output), whose value corresponds to 0.5 LSB to the A/D Channel 0.

3. Adjust VR3 until the reading of A/D flickers between 0 and 1.

4. Connect a DC voltage source (D/A output), whose value corresponds to 4094.5 LSB to the A/D channel 0.

5. Adjust VR2 until the reading of A/D flickers between 4094 and 4095.

6. Repeat step 2 to step 5 to adjust VR2 and VR3.

7. Select unipolar input configuration. Connect a DC voltage source (D/A output) whose value corresponds to 0.5 LSB to the A/D channel 0. Adjust VRI until the reading of A/D flickers between 0 and 1.

D.3. D/A Calibration

A reference voltage within the range ±10V should be connected to the reference input of the D/A channel to be calibrated. Either the on-board -5 V (-10 V) reference or an external reference may be used. The zero offset and full scale gain of the D/A channel can be adjusted with VR6 and VR5 respectively. A precision voltmeter should be used to calibrate the D/A output.

1. Set the D/A data to 0, and adjust VR6 until the D/A output voltage measures 0 volts.

2. Set the D/A data to 4095, and adjust VR5 until the D/A output voltage equals the reference voltage minus 1 LSB, but with the opposite sign; for example, if V_{ref} = -5 V, then V_{out} = +4.9988 V.

–END-