WITIO-PCIe192
STANDARD

EDP-Nr.: A-864600

192 Inputs/Outputs

wasco®

user‘s guide

wasco®

Registered Trademarks

BASIC is a registered trademark of Dartmouth College.
Windows is a registered trademark of Microsoft.
wasco® is registered trademark.

Disclaimer

The company Messcomp Datentechnik GmbH assumes no liability for the use of the interface card WITIO-PCIe192STANDARD and this documentation, neither for direct nor indirect damages.

wasco®

Table of Contents

1. Description

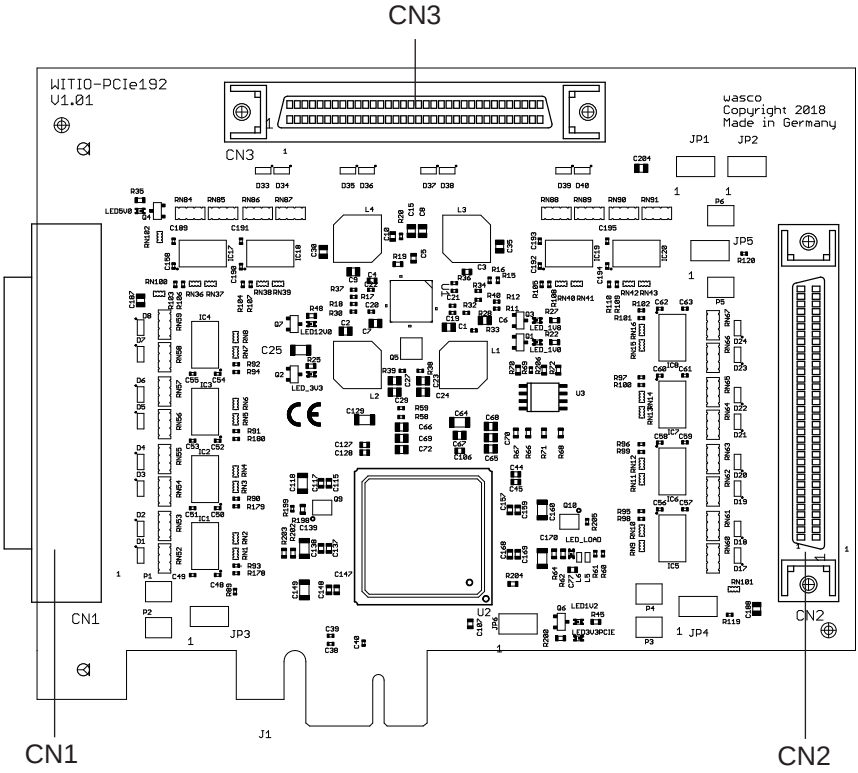
The **wasco**® interface card WITIO-PCIe192STANDARD (Boardname: WASCO-PCIe8182) provides 192 digital input or output channels. You can adjust 3,3V or 5V input and output levels by setting jumpers. This card is suitable for input and output applications not requiring galvanic isolation. The 192 input/output channels are programmable to be input or output in groups of eight channels each. The internal data bus of this card is 32 bits organized, each read / write access to the inputs and outputs is 32-bit access. One 68-pin SCSI socket on the slot plate of the board and two 68-pin SCSI sockets with 64 channels each allow connection to the peripherals.
The pin assignments of all the connectors of the WITIO-PCIe192STANDARD are in compatibility mode identical to the the assignments of the PCI bus cards WITIO-PCI32STANDARD and WITIO-PCI64EXTENDED. A migration to PCIe is thus easily feasible.

2. Installation of the WITIO-PCIe192STANDARD

2.1 Installation of the card into your system

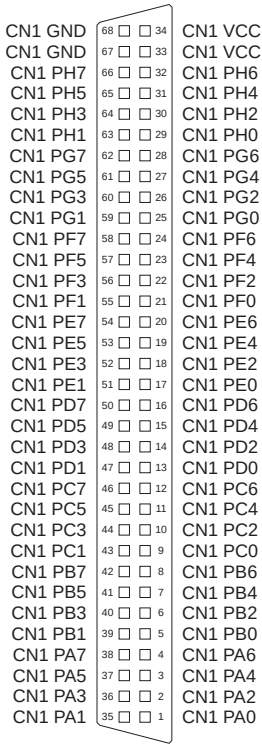
Before you insert the WITIO-PCIe192 unplug the power cord or make sure, there is no current to/in the computer. Inserting into a running system may cause damaging or destroying not only WITIO-PCIe192, but even other already inserted cards of your computer.
Select a free PCIe slot of your computer for then inserting the card. Please refer to the computer‘s manual for support. Screw the slot plate of the board to the computer housing to avoid a card‘s coming loose during operation by effects of the cables.

3. Connectors



CN1: 64 TTL I/Os
CN2: 64 TTL I/Os
CN3: 64 TTL I/Os

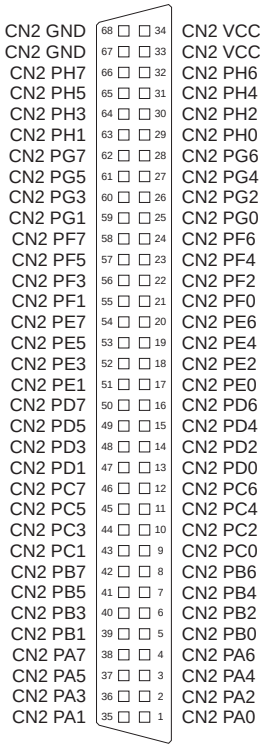
3.2 Pin assignment of CN1



Vcc:
Internal voltage supply (+ 5V / +3,3V) of the PCIe card (configurable by JP3),
Never apply an external voltage across this pin.

GND:
Ground connection

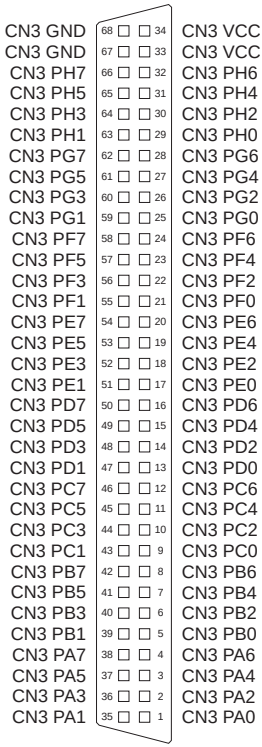
3.3 Pin assignment of CN2



Vcc:
Internal voltage supply (+ 5V / +3,3V) of the PCIe card (configurable by JP4),
Never apply an external voltage across this pin.

GND:
Ground connection

3.4 Pin assignment of CN3

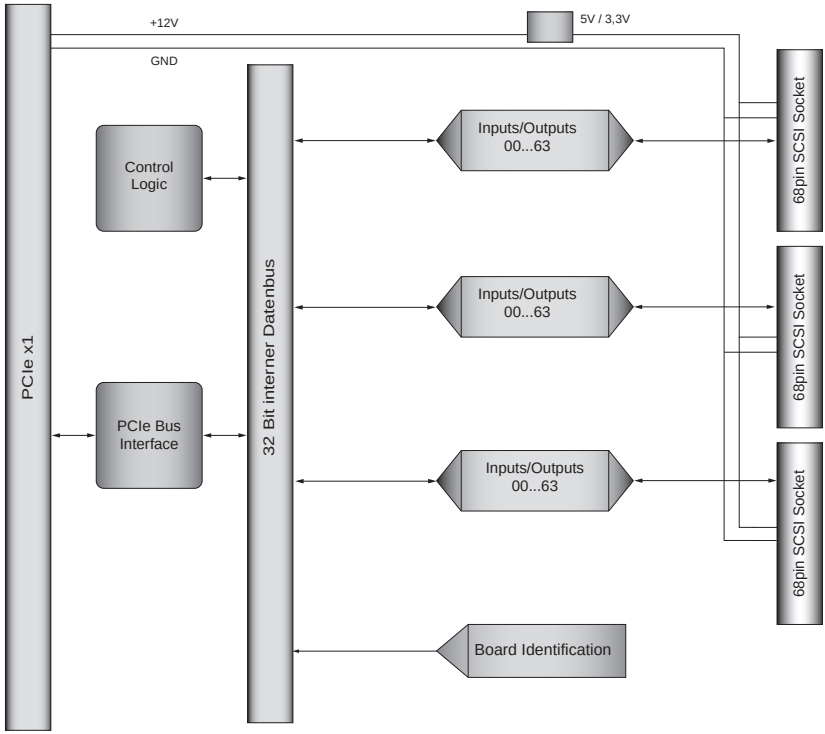


Vcc:
Internal voltage supply (+ 5V / +3,3V) of the PCIe card (configurable by JP5),
Never apply an external voltage across this pin.

GND:
Ground connection

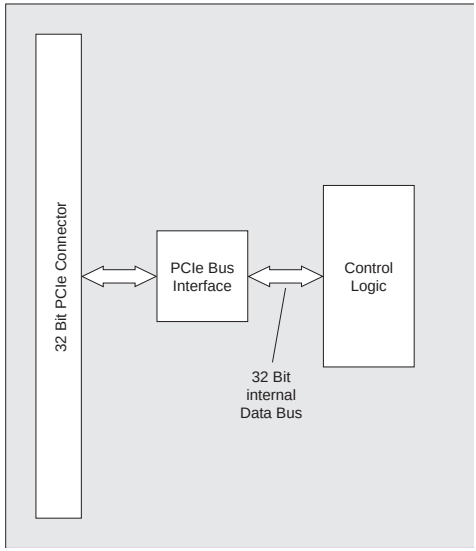
4. System Components

4.1 Block diagram



4.2 Access to the system components

The hardware components of the WITIO-PCIe192 are accessed by reading and writing in Memory Mapped I/O addresses using library functions. The addresses relevant to the WITIO-PCIe192 depend on a base address assigned by the BIOS. You can access to the WITIO-PCIe192 exclusively in double word access. (Please find more information on this topic in the chapter Programming or in example programs on the supplied CD)



5. 192 Digital Inputs / Outputs

For digital input / output, the WITIO-PCIe192Standard provides three identically constructed connectors with 64 digital IOs each.
These 64 digital IOs are arranged in groups of eight channels each (PortA to PortH). You can configure the direction (input or output) of each port individually via a register access. You can set the input / output level (3.3V/5V) of each connector by setting a jumper.

5.1 Selection of the Direction

The port direction of a connector can be defined by writing to the direction register (DDIRCN1, DDIRCN2 or DDIRCN3). Each bit of the register represents a port of the connector. In the default state, all of the ports are defined to be input (except during compatibility mode).
If the corresponding bit is written 1, the corresponding port is configured as input port, with a 0 as output port.

5.2 Read Inputs

For reading the inputs, always 32 IOs (4 ports) are joined in a 32-Bit register (DIN0CN1, DIN1CN1, DIN0CN2, DIN1CN2, DIN0CN3, DIN1CN3). If not all of the register ports are configured as input, the corresponding areas in the register are undefined and can be hidden in the application program using an AND operation.

0 = LOW at the input pin
1 = HIGH at the input pin

5.3 Read / Write outputs

Writing to the register DOUTyCNx sets the outputs. Each connector has two of these registers (DOUT0CNx und DOUT1CNx), in each of which 32 IO pins (4 ports) join together. If not all of the register ports are configured as output, then only the output ranges in the register are taken into account by the card.

0 = LOW at the output pin (if configured as output)
1 = HIGH at the output pin (if configured as output)

5.4 Deactivation of ports

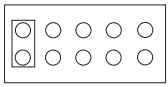
In order to minimize the power consumption of the card, and to prevent possible interferences on the connector, not used ports and their IOs can be deactivated. If a port is deactivated, all of the IOs are high-impedance. Ports always can be deactivated two by two, that is 16-channel-wise. To do this, set the respective bit of the DENCNx.

0 = port group activated
1 = port group deactivated

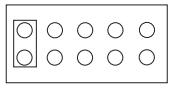
(y = Register number, x = Connector number)

5.5 Level Adjustment

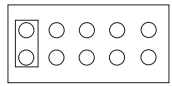
You can configure the voltage level for each of the connectors (IOs and VCC-PINs) with +3.3V and +5V. This is done by setting a jumper on the jumper block of the corresponding connector.



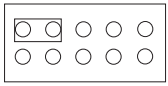
JP3 Voltage Level
CN1 +3.3V



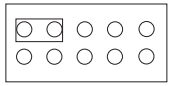
JP4 Voltage Level
CN2 +3.3V



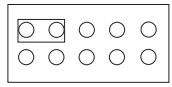
JP5 Voltage Level
CN3 +3.3V



JP3 Voltage Level
CN1 +5V



JP4 Voltage Level
CN2 +5V

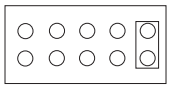


JP5 Voltage Level
CN3 +5V

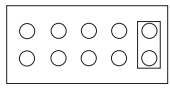
5.6 IOs in Compatibility Mode

If required, each of the connectors can operate in compatibility mode. In this mode, the pinout corresponds to the pinout of the cards WITIO-PCI32$_{\text{Standard}}$ and WITIO-PCI64$_{\text{Extended.}}$ Then, the first 32 IO pins are configured as inputs and the second 32 IO pins as outputs.

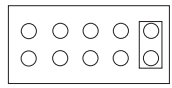
For using the compatibility mode of a connector, you have to set the jumper of the respective jumper block as shown below. The registers DDIRCNx are disabled in the case of the compatibility mode.



JP3 Compatibility Mode
CN1



JP4 Compatibility Mode
CN2



JP5 Compatibility Mode
CN3

5.7 Port Addresses

Offset Address	Register Name	Bit Range	Bits																	
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
0x140	DIN0CN1	31:16	DIN0CN1 <31:16>															
		15:0	DIN0CN1 <15:0>															
0x144	DIN1CN1	31:16	DIN1CN1 <31:16>															
		15:0	DIN1CN1 <15:0>															
0x148	DIN0CN2	31:16	DIN0CN2 <31:16>															
		15:0	DIN0CN2 <15:0>															
0x14C	DIN1CN2	31:16	DIN1CN2 <31:16>															
		15:0	DIN1CN2 <15:0>															
0x150	DIN0CN3	31:16	DIN0CN3 <31:16>															
		15:0	DIN0CN3 <15:0>															
0x154	DIN1CN3	31:16	DIN1CN3 <31:16>															
		15:0	DIN1CN3 <15:0>															
0x160	DOUT0CN1	31:16	DOUT0CN1 <31:16>															
		15:0	DOUT0CN1 <15:0>															
0x164	DOUT1CN1	31:16	DOUT1CN1 <31:16>															
		15:0	DOUT1CN1 <15:0>															
0x168	DOUT0CN2	31:16	DOUT0CN2 <31:16>															
		15:0	DOUT0CN2 <15:0>															
0x16C	DOUT1CN2	31:16	DOUT1CN2 <31:16>															
		15:0	DOUT1CN2 <15:0>															
0x170	DOUT0CN3	31:16	DOUT0CN3 <31:16>															
		15:0	DOUT0CN3 <15:0>															
0x174	DOUT1CN3	31:16	DOUT1CN3 <31:16>															
		15:0	DOUT1CN3 <15:0>															

Offset-Adresse	Register Name	Bit Range	Bits																				
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
0x180	DDIRCN1	31:16	reserved (*)															
		15:0	reserved (*)											DDIRCN1 <7:0>				
0x184	DDIRCN2	31:16	reserved (*)															
		15:0	reserved (*)											DDIRCN2 <7:0>				
0x188	DDIRCN3	31:16	reserved (*)															
		15:0	reserved (*)											DDIRCN3 <7:0>				
0x190	ENCN1	31:16	reserved (*)															
		15:0	reserved (*)													ENCN1 <3:0>		
0x194	ENCN2	31:16	reserved (*)															
		15:0														ENCN2 <3:0>		
0x198	ENCN3	31:16	reserved (*)															
		15:0	reserved (*)													ENCN3 <3:0>		

(*) reserved area has to be assigned 0

Register DIN0CNx (x = number of the connector):

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R							
	DIN0CNx <31:24> (PD7 : PD0)							
23:16	R							
	DIN0CNx <23:16> (PC7 : PC0)							
15:8	R							
	DIN0CNx <15:8> (PB7 : PB0)							
7:0	R							
	DIN0CNx < 7:0> (PA7 : PA0)							

Bit 31 - 24 DIN0CNx <31:24> Port D Inputs PD7 to PD0 of the connector
Bit 23 - 16 DIN0CNx <23:16> Port C Inputs PC7 to PC0 of the connector
Bit 15 - 8 DIN0CNx <15:8> Port B Inputs PB7 to PB0 of the connector
Bit 7 - 0 DIN0CNx <7:0> Port A Inputs PA7 to PA0 of the connector

Register DIN1CNx (x = number of the connector):

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R							
	DIN1CNx <31:24> (PH7 : PH0)							
23:16	R							
	DIN1CNx <23:16> (PG7 : PG0)							
15:8	R							
	DIN1CNx <15:8> (PF7 : PF0)							
7:0	R							
	DIN1CNx < 7:0> (PE7 : PE0)							

Bit 31 - 24 DIN1CNx <31:24> Port H Inputs PH7 to PH0 of the connector
Bit 23 - 16 DIN1CNx <23:16> Port G Inputs PG7 to PG0 of the connector
Bit 15 - 8 DIN1CNx <15:8> Port F Inputs PF7 to PF0 of the connector
Bit 7 - 0 DIN1CNx <7:0> Port E Inputs PE7 to PE0 of the connector

Register DOUT0CNx (x = number of the connector):

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W							
	DOUT0CNx <31:24> (PD7 : PD0)							
23:16	R/W							
	DOUT0CNx <23:16> (PC7 : PC0)							
15:8	R/W							
	DOUT0CNx <15:8> (PB7 : PB0)							
7:0	R/W							
	DOUT0CNx < 7:0> (PA7 : PA0)							

Bit 31 - 24 DOUT0CNx <31:24> Port D Inputs PD7 to PD0 of the connector
Bit 23 - 16 DOUT0CNx <23:16> Port C Inputs PC7 to PC0 of the connector
Bit 15 - 8 DOUT0CNx <15:8> Port B Inputs PB7 to PB0 of the connector
Bit 7 - 0 DOUT0CNx <7:0> Port A Inputs PA7 to PA0 of the connector

Register DOUT1CNx (x = number of the connector):

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W							
	DOUT1CNx <31:24> (PH7 : PH0)							
23:16	R/W							
	DOUT1CNx <23:16> (PG7 : PG0)							
15:8	R/W							
	DOUT1CNx <15:8> (PF7 : PF0)							
7:0	R/W							
	DOUT1CNx < 7:0> (PE7 : PE0)							

Bit 31 - 24 DOUT1CNx <31:24> Port H Inputs PH7 to PH0 of the connector
Bit 23 - 16 DOUT1CNx <23:16> Port G Inputs PG7 to PG0 of the connector
Bit 15 - 8 DOUT1CNx <15:8> Port F Inputs PF7 to PF0 of the connector
Bit 7 - 0 DOUT1CNx <7:0> Port E Inputs PE7 to PE0 of the connector

Register DDIRCNx (x = number of the connector):

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U							
	reserved							
23:16	U							
	reserved							
15:8	U							
	reserved							
7:0	R/W							
	DDIRCNx <7:0>							

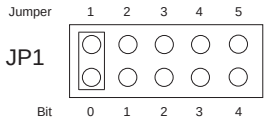
Bit 31 - 8 reserved (value 0 is to be written)
Bit 7 - 0 DDIRCNx <7:0> (default = 1)
0 = IO PIN configured as output
1 = IO PIN configured as input
DDIRCNx <0> = Port A, DDIRCNx <1> = Port B,
DDIRCNx <2> = Port C, DDIRCNx <3> = Port D,
DDIRCNx <4> = Port E, DDIRCNx <5> = Port F,
DDIRCNx <6> = Port G, DDIRCNx <7> = Port H

Register DENCNx (x = number of the connector):

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U							
	reserved							
23:16	U							
	reserved							
15:8	U							
	reserved							
7:0	U				R/W			
	reserved				DENCNx <3:0>			

Bit 31 - 4 reserved (value 0 is to be written)
Bit 3 - 0 DENCNx <3:0> (default = 0)
0 = enable port groups
1 = disable port groups
DENCNx <0> = Port A + Port B
DENCNx <1> = Port C + Port D
DENCNx <2> = Port E + Port F
DENCNx <3> = Port G + Port H

6. Board Identification



The board identification is used to differentiate between several PC cards of the same type on the computer. This is done by a jumper block, which can be read by software.

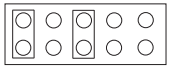
The board identification to be read consists of one Byte (8 Bit) and is structured as follows:

Bit	7	6	5	4	3	2	1	0
Jumper				5	4	3	2	1
Board ID Register	0	0	0	x	x	x	x	x

„x“ is „1“, if the jumper is set, otherwise „0“

The jumper setting of the jumper block JP1 can be read out by means of the read command. The unused bits are basically „0“, a set jumper is read as „1“.

E.g

JP1  (Jumper 1 and 3 set)

Result of the read command: $05

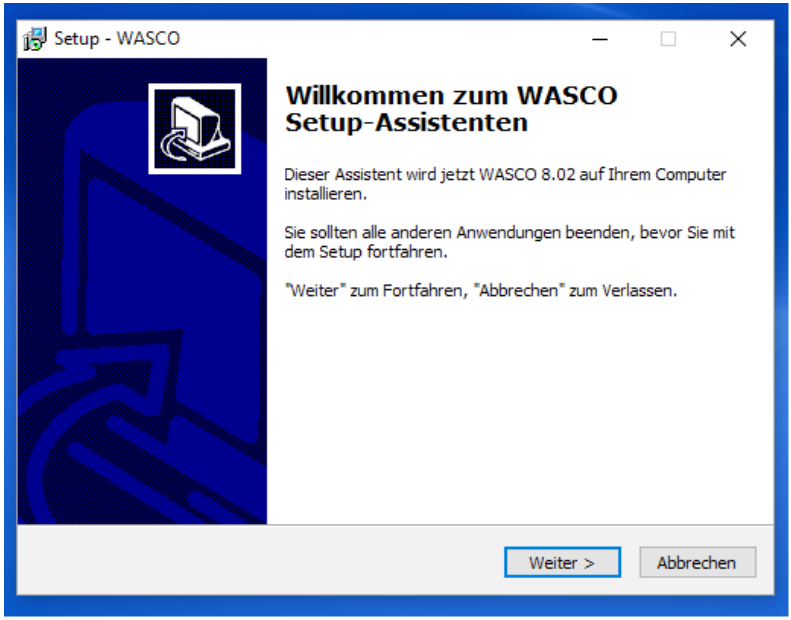
7. Programming under Windows®

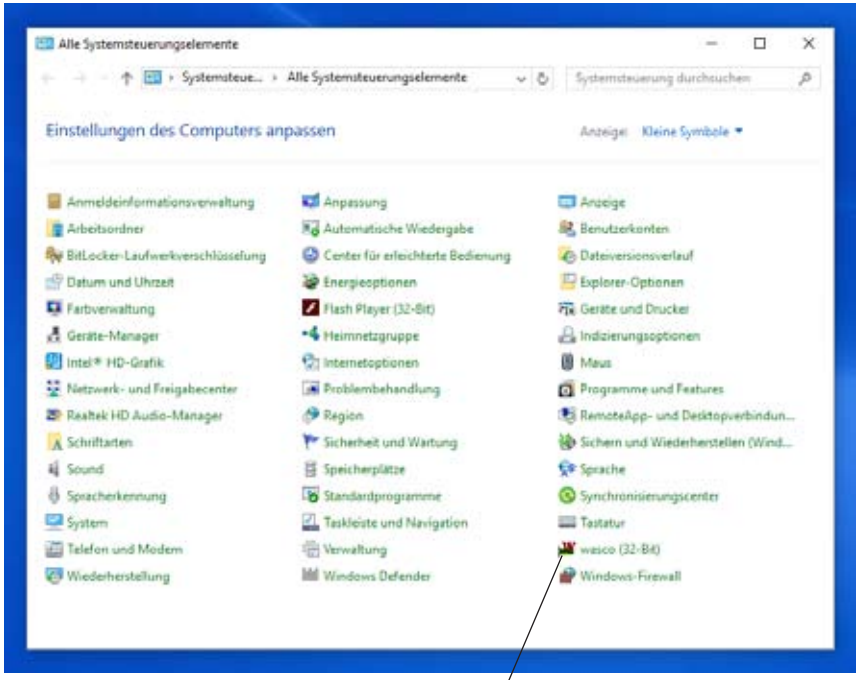
7.1 Installation of the Windows® driver

In order to implement the card under Windows®, it is necessary to install a special driver, which allows access to the card. The operating system under Windows® 10, 8 and 7 automatically reports after starting the PC, that a new hardware component has been found. In this case, insert the data medium and instruct to the system to install the driver files herefrom. If the operating system does not respond, the driver also can be installed in the Device Manager.

7.2 Installation of the Windows® development files

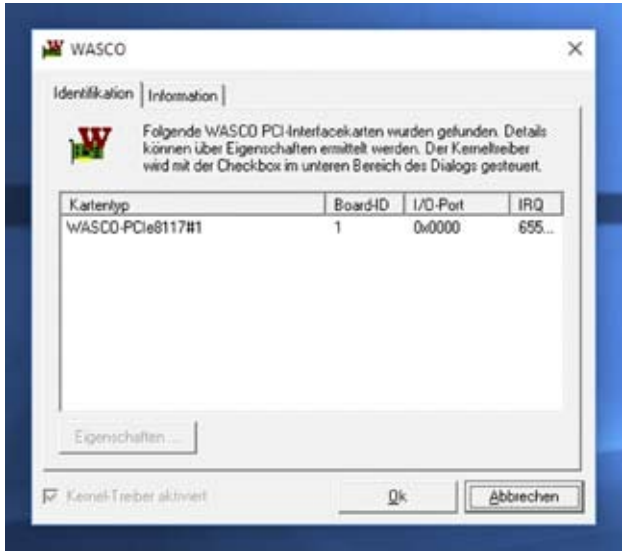
For installation of the development files, please run the file „Setup.exe“ in the folder driver on the accompanying CD and follow the installation instructions.





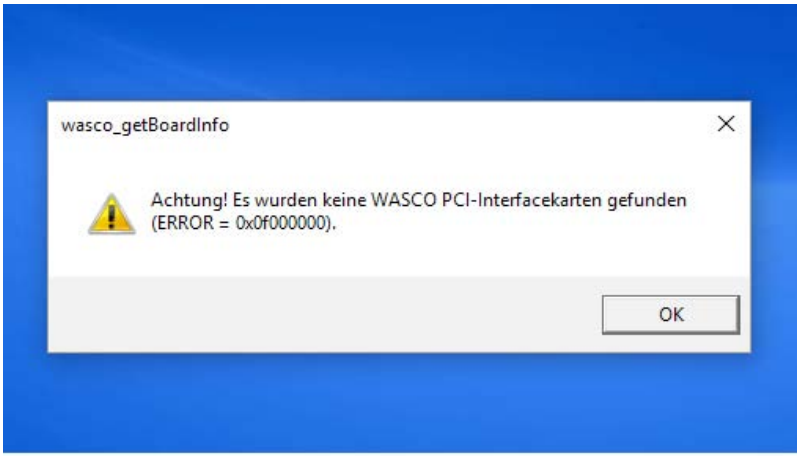
Once the driver and development files have been installed completely, you will find an icon in the control panel of your computer to localize all **wasco**® PCI and PCIe cards available in the system.

Start the card query by double clicking on the "wasco®" Icon. The following window appears (A WASCO-PCIe8117 was used here as an example)



If your card has been detected in the system, the board name WASCO-PCIe8182, Board-ID, I/O address as well as the possible interrupt number of the respective card are displayed in this window. Furthermore, the driver version and the location of the driver file can be queried via the „Information“ tab.

If your card was not detected, following error message will be displayed:



Please find more about the possible causes in the chapter Troubleshooting.

7.3 Programming the WITIO-PCIe192 with wasco® driver

After installing development files of Kithara by means of the setup program the folder .../**wasco**/ contains of the relevant development files and the sample programs. Further sample programs specified for access to the WITIO-PCIe192, you can find on the enclosed CD or please visit our homepage.

Programming the hardware components of the WITIO-PCIe192 is realized by access to Memory Mapped I/O addresses which depend on the base address assigned by the system‘s BIOS for the WITIO-PCIe192. Find a more detailed description for programming in the driver documentation.

7.4 Assignment of the Memory Mapped I/O Addresses

The Memory Mapped I/O addresses of the single hardware components depend on the base address, as shown in following table using a few examples:

Port/Register	BA + Offset	RD/WR
read first 32 inputs of CN1 (PD7..PD0, PC7..PC0, PB7..PB0, PA7..PA0)	BA + $140	RD
read second 32 inputs of CN1 (PH7..PH0, PG7..PG0, PF7.F0, PE7..PE0)	BA + $144	RD
read/write first 32 outputs of CN1 (PD7..PD0, PC7..PC0, PB7..PB0, PA7..PA0)	BA + $160	RD/WR
read/write second 32 outputs of CN1 (PH7..PH0, PG7..PG0, PF7.F0, PE7..PE0)	BA + $164	RD/WR
Board Identification	BA+ $3E0	RD

7.5 Compatibility with WITIO-PCI32Standard and WITIO-PCI64Extended

When developing the WITIO-PCIe192Standard special attention was paid to the easiest possible migration of the WITIO-PCI32Standard and WITIO-PCI64Extended. For this purpose, the pin assignment of the CN1, CN2 and CN3 matches to those of the two PCI cards, upon need. To migrate in a very simple way, set the compatibility jumper of the respective connector (see chapter 5.6). This defines the first 32 IOs of the connectors as inputs and the second 32 IOs as outputs. In this mode, the direction register has no effect on the direction of the IOs.

What has changed or what needs to be changed for PCIe board:

1. The board name is „WASCO-PCIe8182“
2. The functions to access to the port addresses for the PCIe board are „wasco_outputPCIeD“ and „wasco_inputPCIeD“
3. The offsets to access to the Memory Mapped I/O addresses have changed

TTL input portA (DIN00...31)	BA + $140 (CN1)
	BA + $148 (CN2)
	BA + $150 (CN3
TTL output portB (DOUT00...31)	BA + $164 (CN1)
	BA + $160 (CN2)
	BA + $174 (CN3)

   (Unchanged constants are usable for PCI cards only).

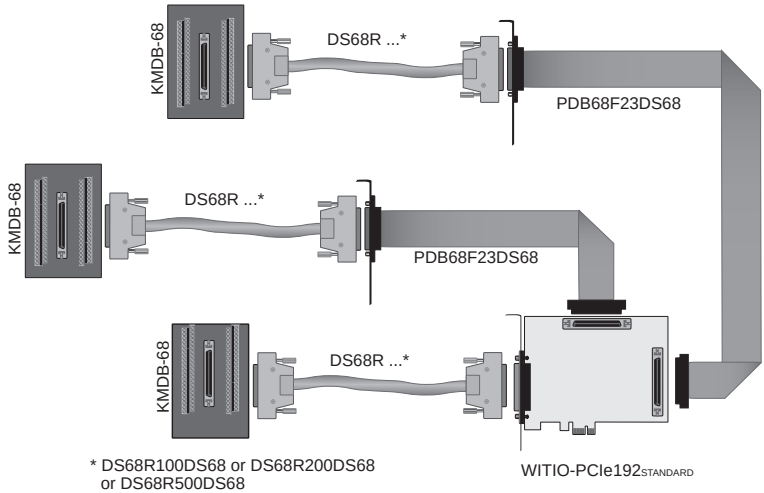
4. The setting of jumper block JP1 can be queried via an additional address. The jumper can be used, for example, for the identification of the WITIO-PCIe192STANDARD in case your computer registers several cards in the PC.

8. Accessories

8.1 Compatible wasco® accessories

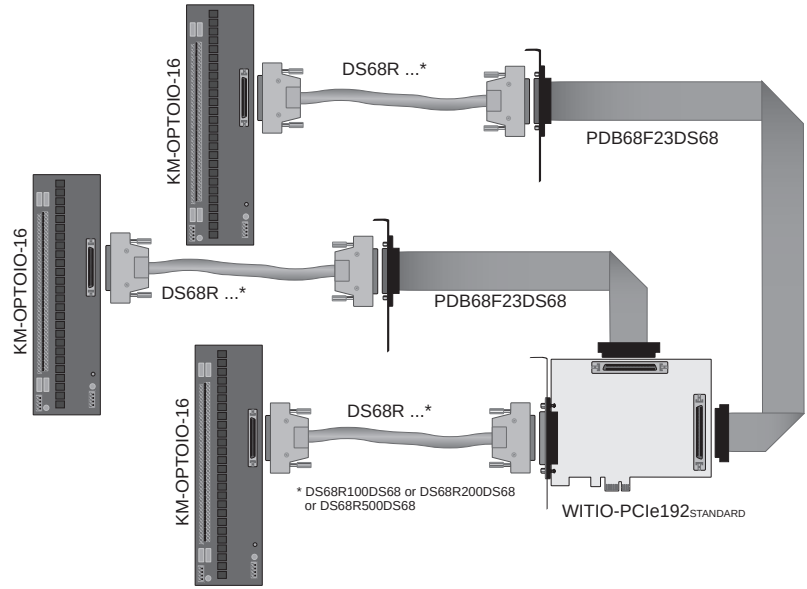
Connecting parts	EDP No.
PDB68F23DS68 Plugged ribbon cable	A-498500
DS68R200DS68 Connecting wire (2 meters)	A-492400
DS68R500DS68 Connecting wire (5 meters)	A-492800
KMDB-68 Connecting Board	A-494800
KM-OPTOIN-32 Optocoupler module	A-483600
KM-OPTOOUT-32 Optocoupler module	A-484600
KM-PREL-16 Relais module	A-485400
KM-REL-8 Relais module	A-486200
KM-VB-5 Connection module	A-488200

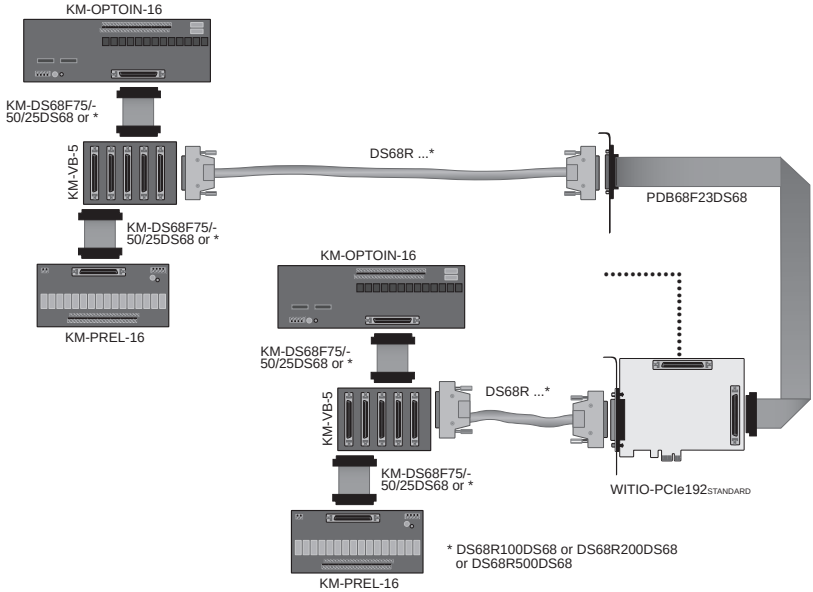
8.2 Connecting technique (application examples)

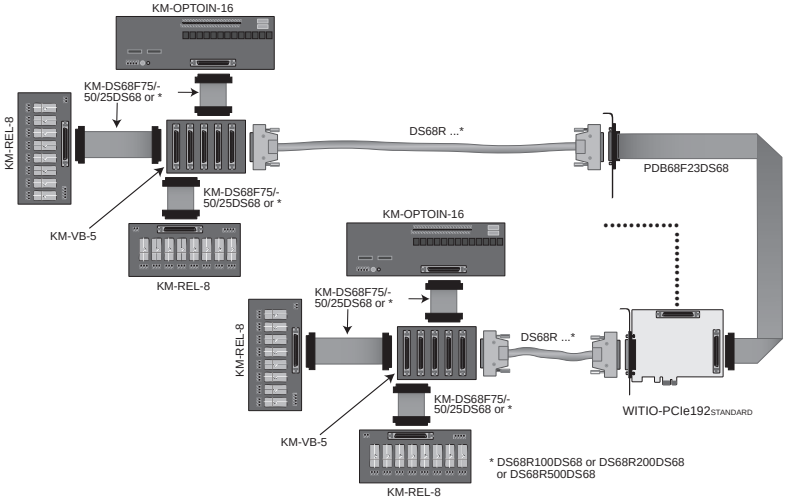


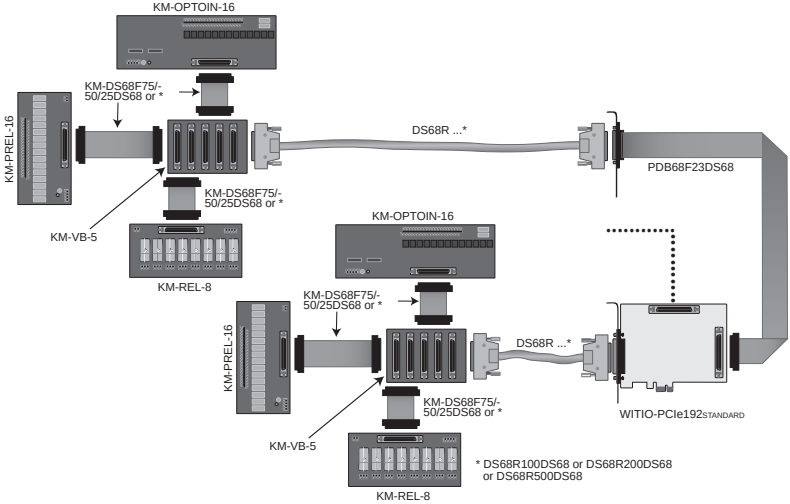
* DS68R100DS68 or DS68R200DS68 or DS68R500DS68

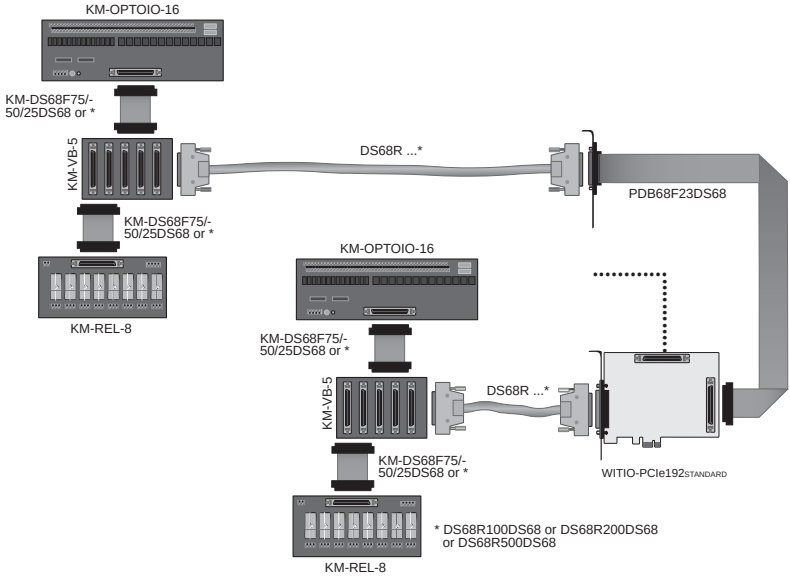
WITIO-PCIe192STANDARD

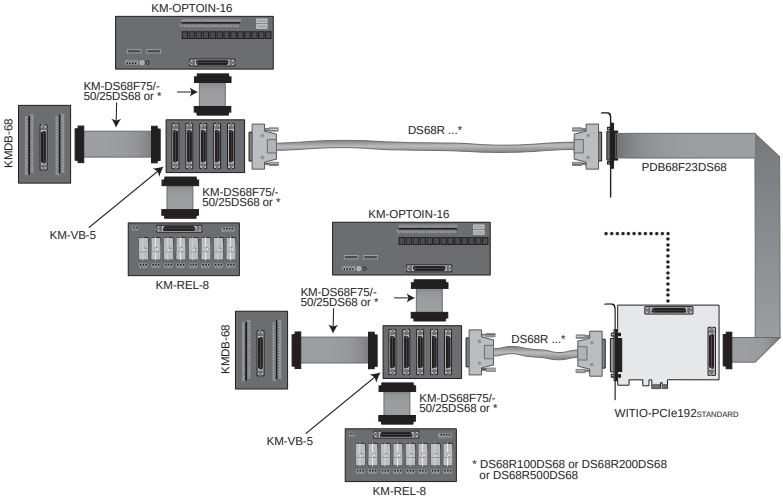

KM-OPTOIO-16
DS68R ...*
PDB68F23DS68
KM-OPTOIO-16
DS68R ...*
PDB68F23DS68
KM-OPTOIO-16
DS68R ...*
* DS68R100DS68 or DS68R200DS68
or DS68R500DS68
WITIO-PCIe192STANDARD


KM-OPTOIN-16
KM-DS68F75/-
50/25DS68 or *
KM-VB-5
DS68R ...*
PDB68F23DS68
KM-DS68F75/-
50/25DS68 or *
KM-PREL-16
KM-OPTOIN-16
KM-DS68F75/-
50/25DS68 or *
KM-VB-5
DS68R ...*
KM-DS68F75/-
50/25DS68 or *
WITIO-PCIe192STANDARD
* DS68R100DS68 or DS68R200DS68
or DS68R500DS68
KM-PREL-16


KM-OPTOIN-16
KM-DS68F75/-
50/25DS68 or *
KM-REL-8
DS68R ...*
PDB68F23DS68
KM-DS68F75/-
50/25DS68 or *
KM-VB-5
KM-REL-8
KM-OPTOIN-16
KM-DS68F75/-
50/25DS68 or *
KM-REL-8
DS68R ...*
KM-DS68F75/-
50/25DS68 or *
KM-VB-5
WITIO-PCIe192STANDARD
KM-REL-8
* DS68R100DS68 or DS68R200DS68
or DS68R500DS68


KM-OPTOIN-16
KM-DS68F75/-
50/25DS68 or *
KM-PREL-16
DS68R ...*
PDB68F23DS68
KM-DS68F75/-
50/25DS68 or *
KM-VB-5
KM-REL-8
KM-OPTOIN-16
KM-DS68F75/-
50/25DS68 or *
KM-PREL-16
DS68R ...*
KM-DS68F75/-
50/25DS68 or *
KM-VB-5
WITIO-PCIe192STANDARD
KM-REL-8
* DS68R100DS68 or DS68R200DS68
or DS68R500DS68


KM-OPTOIO-16
KM-DS68F75/-
50/25DS68 or *
KM-VB-5
DS68R ...*
PDB68F23DS68
KM-DS68F75/-
50/25DS68 or *
KM-REL-8
KM-OPTOIO-16
KM-DS68F75/-
50/25DS68 or *
KM-VB-5
DS68R ...*
KM-DS68F75/-
50/25DS68 or *
WITIO-PCIe192STANDARD
KM-REL-8
* DS68R100DS68 or DS68R200DS68
or DS68R500DS68


KM-OPTOIN-16
KM-DS68F75/-
50/25DS68 or *
KMDB-68
DS68R ...*
PDB68F23DS68
KM-DS68F75/-
50/25DS68 or *
KM-VB-5
KM-REL-8
KM-OPTOIN-16
KM-DS68F75/-
50/25DS68 or *
KMDB-68
DS68R ...*
KM-DS68F75/-
50/25DS68 or *
WITIO-PCIe192STANDARD
KM-VB-5
* DS68R100DS68 or DS68R200DS68
or DS68R500DS68
KM-REL-8

8.3 Component parts for customized assembly

Connection parts	EDP-No.
SCSI-II plug 68-pin for flat ribbon cable	A-553200
SCSI-II socket 68-pin for flat ribbon cable	A-557200
SCSI-II plug 68-pin for solder connection	A-555340
Slot plate with cutout for male/female connector 68-pin	A-577800
Flat ribbon cable 68-pin	A-572800

9. Troubleshooting

Following you can find a brief compilation of the most common known causes of errors that may occur during starting-up or while running the WITIO-PCIe192.
Please check these points before you contact your dealer or distributor to solve your problem:

1st	Is WITIO-PCIe192 properly inserted to the connector ?
2nd	Are all cable connections all right?
3rd	Did your system detect the card correctly? Please check all settings of your computer or contact your system administrator. (As this are BIOS settings of the computer we cannot expand on this issue. We refer to your system manual.)
4th	Did you install the latest driver version for the wasco® drivers? Updates you can find here: http://www.messcomp.com

10. Specifications

Inputs / Outputs
Channels: 192
Output level 3.3V/5V, adjustable by jumpers
Output current: 5 mA per channel
Programmable in 8-Bit-groups as input or output

Connection plug
3 * 68pin SCSI socket

Bus system
32 Bit PCIe-Bus
(Internal Data access 32Bit)

Dimensions of the board
137 mm x 111 mm (l x h)

Others
Protection and Control LEDs for power supply

11. Product Liability Act

Information on Product Liability

The Product Liability Act (Act on Liability for Defective Products - ProdHaftG) in Germany regulates the manufacturer‘s liability for damages caused by defective products.

The obligation to pay compensation may already exist, if the product’s presentation could cause a misconception of safety to a non-commercial end-user and also if the end-user is expected not to observe the necessary safety instructions when handling this product.

It must therefore always be shown, that the non-commercial end-user was made familiar with the safety rules.

In the interest of safety, please always advise your non-commercial customers of the following safety instructions:

Safety Instructions

The valid VDE regulations must be observed, when handling products that come into contact with electrical voltage.

Particular attention must be paid to the regulations:
VDE100; VDE0550/0551; VDE0700; VDE0711; VDE0860.

You recieve the VDE regulations at:
Vde-Verlag GmbH
Bismarckstr. 33
10625 Berlin
Germany

* unplug the power plug before you open the unit or make sure, there is no current to/in the unit.

* You only may start up any components, boards or equipment, if they have been installed in a touch-proof casing before. During installation, the the equipment must be de-energized.

* Make sure that the device is disconnected from the power supply before using any tools on any components, boards or equipment. Any electric charges stored in components in the device are to be discharged prior.

* Live cables or wires, which are connected with the unit, the components or the boards, must be examined for insulation faults or breaks. In case of any defect the device must be taken out of service immediately, until the defective lines have been replaced.

* When using components or circuit boards you must strictly comply with the characteristic specifications for electrical parameters stated in the relevant description.

* As a non-commercial end-user, if it is not clear whether or not the electrical characteristic specifications given in the provided description apply to a component, you must consult a specialist.

Furthermore, the compliance with construction and safety regulations of all kinds (VDE, TÜV, industrial injuries corporation, etc.) is subject to the user/customer.

12. Declaration of Conformity

This is to certify, that the CE marked product

WITIO-PCIe192STANDARD
EDP Number A-864600

comply with the requirements of the relevant EMC directives 2014/30/EU. This declaration will lose its validity, if the instructions given in this manual for the intended use of the products are not fully complied with.

The following standards were considered:

EN 55011: 2009 + A1. 2010 (Group 1, Class A)
EN 55022: 2010 / AC: 2011
EN 55024: 2010
EN 61000-6-4: 2007 + A1: 2011
EN 61000-6-2: 2005 / AC: 2005
(EN 6100-4-2: 2008; EN 6100-4-3: 2006 + A1: 2007 + A2; EN 6100-4-4: 2012; EN 6100-4-5: 2014; EN 6100-4-6: 2013; EN 6100-4-8: 2009; EN 6100-4-11: 2004)

The following manufacturer is responsible for this declaration:

Messcomp Datentechnik GmbH
Neudecker Str. 11
83512 Wasserburg

submitted by

Dipl.Ing.(FH) Hans Schnellhammer

Wasserburg, 26.09.2017

Reference system for intended use

This PC expansion card is not a stand-alone device. The CE-conformity only can be assessed when using additional computer components simultaneously. Thus the information to the CE conformity exclusively refers to the following reference system for the intended use of the PC expansion card:

Control Cabinet:	Vero IMRAK 3400	804-530061C 802-563424J 802-561589J
19“ Casing:	Vero PC Casing	145-010108L
19“ Casing:	Additional Electronics	519-112111C
Motherboard:	ASUS P5G41-M LE	
Interface:	WITIO-PCIe192$_{STANDARD}$	A-864600